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Procedure for Minimizing the Cost Per Watt of Photovoltaic Systems*

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Abstract—A general analytic procedure is developed that provides the first quantitative method for optimizing any element or process in the fabrication of a photovoltaic energy conversion system by minimizing its impact on the cost per Watt of the complete system. By determining the effective value of any power loss associated with each element of the system, this procedure furnishes the design specifications that optimize the cost-performance tradeoffs for each element. A general equation is derived that optimizes the properties of any part of the system in terms of appropriate cost and performance functions, although the power-handling components are found to have a different character from the cell and array steps. Another principal result of this analysis is that a fractional performance loss occurring at any cell- or array-fabrication step produces that same fractional increase in the cost per Watt of the complete array (although not in the power-handling components), thus quantifying an intuitively sensed effect. It also follows that no element or process step can be optimized correctly by considering only its own cost and performance. Some other solar-energy conversion systems that contain analogous classes of components appear to also be amenable to this type of analysis.

Introduction

Optimization of solar-cell design characteristics for satellite systems has utilized as its criterion the maximum power output[1] and, occasionally, the weight of the devices. In space applications cost considerations had

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to be suppressed. Photovoltaic systems for terrestrial uses, however, have as their central goal cost reduction. Since this must be achieved without excessive loss in performance, there is a need for some quantitative means of optimizing the cost versus performance tradeoffs. That need is met by the procedure described in this paper whose optimization criterion is the minimum cost/Watt of the complete system. Further, such optimization should be capable of being performed for every step in the fabrication process of the active converter as well as for every other system element. Although there are formal optimization methods for dealing with such problems, the present analysis is carried out in a way that emphasizes physical insight rather than abstract theory.

This procedure is based on the (generally valid) hypothesis that the entire fabrication process—from raw materials to system completion—can be represented by a sequence of basically independent "steps". This independence must apply to both the cost and performance aspects of the various steps. For cases in which some steps interact strongly with others, they must be grouped together to form a composite "step" for the purposes of analysis. (This statement is true, of course, for other analytical methods as well.) The meaning of this independence requirement will be shown in the subsequent discussion.

To permit analysis of the fabrication costs, we consider cost elements of the system in several classes: (1) steps associated with the fabrication of the active solar cells; (2) steps associated with the collector array—of which the "module" is the representative unit—including its structure; (3) system elements that process the generated power; and (4) fixed costs not directly allocable to any of these steps (factory-level overhead, manufacturers' profit, etc.). It is vital to successful optimization of the system that these classes be properly distinguished in the evaluation of their cost contributions, since they enter as groups in different ways.

The optimization analysis could be carried out by either of two approaches: (1) specify some fixed output power level for the system and determine necessary changes in size of the array and of the power-processing elements as some variable of a fabrication step is changed; or (2) fix the array size and determine how the output power level varies under such a change. In either case, the quantity of ultimate concern is the cost/Watt, U, of the output power and the procedure must be able to minimize U. For this purpose we shall not be concerned with the question of whether peak power or average power is to be used; either one can be used, provided the relation between them is known.

This procedure follows the second approach because it simplifies the evaluation of the costs of the numerous cell and array steps, so the collector array area is fixed at A_a. The cell and module fabrication processes

must supply the number of modules needed to cover this area, with provision made for all process yield losses up to and including the completion of array assembly. Past the array completion step (which includes the structure and its foundation), physical yield losses do not occur, but the power level may be attenuated.

The essential feature of this procedure is that it develops a way of allocating *all* system costs to a proportional part of the collector array area A_a. The method for accomplishing this allocation will be shown; the result is that we can write the total cost per Watt U as

$$U = \frac{K}{G_o}, \qquad [1]$$

where K is the total system cost per unit of collector area and G_o is the system output power per unit of collector area.

Evaluation of Performance Factors

The establishment of the output power density G_o in terms of the effects due to individual steps is straightforward. We assign to each step a dimensionless "performance factor" f_j that is defined as the fraction of the potentially available power before step j that is actually obtained after it. In most cases $f_j < 1$, but for certain steps the potentially available power must be chosen arbitrarily so that $f_j > 1$ is then possible. (For example, if the "available power" expectation is based on the use of moderate quality silicon, the use of very good Si can result in better performance.) This does not alter the analysis.

The performance property of central importance in analysis of a photovoltaic power system is that the performance factors of the separate items are *multiplicative* in the full system. That is, the output power density of the system can be expressed as

$$G_o = FG, \qquad [2]$$

where G is the electrical power density potentially available (chosen arbitrarily) and F is the system performance factor. F is given by

$$F = \prod_{j=1}^{n} f_j, \qquad [3]$$

where there are n "steps" in the system fabrication.

By the hypothesized independence of the steps, we may single out any step, say step m, and separate it from the rest of the f_j by a relation

$$F'_m = \frac{F}{f_m}, \qquad [4]$$

where F'_m does not contain the variables of step m.

Evaluation of Cost Terms

The quantitative evaluation of K in Eq. [1] requires a detailed analysis of all four classes of costs in the system fabrication. We first state the major result of this analysis, i.e., that we can express K as a simple sum

$$K = \sum_{j=0}^{n} C_j \qquad [5]$$

where the use of a term labeled C_o is to accommodate all of the fixed costs that are not directly associated with any of the individual steps; the C_j are effective step costs per unit area that include all material costs but are not simply the direct step expenditures. This sum displays one of the properties required for the steps to be independent.

The key to the establishment of Eq. [5] is the correct evaluation of the various types of C_j terms for the different classes of steps described previously. We begin the analysis by identifying the last step involving physical construction of the collector array which we denote as step a. This step will presumably be the mounting of the assembled array onto the support structure, including the making of the required electrical connections. At the completion of step a there are A_a square meters of operational collector ready to deliver power. Assuming the modules cover 100% of this area, then there are A_a m^2 of tested, operating modules. Step a is thus the last one whose costs are proportional to A_a; there is an entire class of such steps beginning with the first module fabrication step after the individual cells have been completed.

The active cells cover a fraction of the module area (and thus of A_a) that we denote as ϕ. If the last step of the cell processing is step c, then all steps up to and including c have costs that can be expressed as being proportional to ϕA_a. Thus two of the four classes of steps are proportional to the area of the collector. The fourth class, fixed costs whose total for the system we call FC, is not directly related to the area so those costs must be added to the total of other system costs. We make the usual assumption that FC is constant for the range of variables permitted.

The third class of steps contains those system elements whose costs are related to their operating power level. This class follows step a and it includes power conditioning equipment, switchgear, and energy storage facilities. In evaluating their costs we must provide for the possible de-

crease in power levels in later system elements due to losses within this class. For this purpose we denote the power density delivered by the array (i.e., after step a) as G_a; this is related to the array conversion efficiency η_a by $G_a = I\eta_a$ where I is the solar irradiance. Then the first power-related element, which we call step p, must operate at the power level A_aG_a. The next element (step $p+1$) operates at power level $f_pA_aG_a$ and so on; at later step j, it is $f_pf_{p+1} \ldots f_{j-1}A_aG_a$. Now each of these power-proportional steps will have a cost that can be written as $u_jf_pf_{p+1} \ldots f_{j-1}A_aG_a$ where $u_j \equiv$ cost per Watt for element j. Now it is seen that these steps too are expressible in terms that are all proportional to A_a.

The total cost of the system T can now be written as

$$\begin{aligned} T = {} & FC && \text{for all the fixed costs} \\ & A_a\left[\frac{k_a}{Y_a} + \frac{k_{a-1}}{Y_aY_{a-1}} + \ldots + \frac{k_{c+1}}{Y_aY_{a-1}\ldots Y_{c+1}}\right] && \text{for array-related costs} \\ & + \phi A_a\left[\frac{k_c}{Y_aY_{a-1}\ldots Y_c} + \ldots + \frac{k_1}{Y_aY_{a-1}\ldots Y_1}\right] && \text{for cell-related costs} \\ & + A_aG_a[u_nf_pf_{p+1}\ldots f_{n-1} + \ldots + u_p] && \text{for power-related steps} \end{aligned} \qquad [6]$$

where $k_j \equiv$ total cost per unit area for performing step j and $Y_j \equiv$ yield of step j. This shows the well-known impact that each yield factor has on all *preceding* steps. Since the cost per unit area of the system is just $K = T/A_a$, we obtain from Eq. [6] the various types of terms C_j to be used in Eq. [5]:

$$C_o = FC/A_a \qquad \text{for fixed costs}$$

$$C_j \equiv \begin{cases} \phi\dfrac{k_j}{Y_aY_{a-1}\ldots Y_j} & \text{for cell steps} \\ \dfrac{k_j}{Y_aY_{a-1}\ldots Y_j} & \text{for array-related steps} \\ G_au_jf_pf_{p+1}\ldots f_{j-1} & \text{for power-related steps.} \end{cases} \qquad [7]$$

With this definition of C_o, the fixed costs associated with the fabrication of the system having collector area A_a can be regarded as simply being allocated over that area.

The C_j's of the power-related steps can be rewritten in another useful

way by substituting for G_a the quantity $G_a = G_o/(f_n f_{n-1} \ldots f_{p+1} f_p)$. Then we find each power-related step cost has the alternative form

$$C_j = G_o \frac{u_j}{f_n f_{n-1} \ldots f_{j+1} f_j}. \qquad [8]$$

Thus, when expressed in terms of the final power density, these terms take on the same form as the cell and array terms but with the performance factors playing the roles of the yields. Indeed, here the f_j's may properly be regarded as "power yields".

This establishes the quantitative values of the terms C_j. By virtue of the independence of these terms, the cost of any step m may be separated from the rest by subtraction, in contrast to the performance factors, so we may define the quantity K'_m, independent of step m, by

$$K'_m = K - C_m. \qquad [9]$$

Optimization Procedure

The minimization of U for the system, given a change in the properties of any step, can be performed by using Eqs. [2] and [5] in Eq. [1]. We shall now see, however, that the power-related steps have a basically different character that requires separate treatment. We write the expression for $K = T/A_a$ adopting an abbreviated notation and using Eq. [8] to express the power-related terms in K

$$K = \frac{FC}{A_a} + \phi \sum_c + \sum_a + G_o \sum_p, \qquad [10]$$

where $\sum_c$ denotes the sum of the cell terms in square brackets of Eq. [6], $\sum_a$ is the sum of array terms in brackets there, and

$$G_o \sum_p \equiv G_o \left[\frac{u_n}{f_n} + \frac{u_{n-1}}{f_n f_{n-1}} + \ldots + \frac{u_p}{f_n f_{n-1} \ldots f_p} \right].$$

Now using Eq. [10] for K in forming $U = K/G_o$ we obtain for the cost/Watt

$$U = \frac{1}{G_o} \left[\frac{FC}{A_a} + \phi \sum_c + \sum_a \right] + \sum_p$$

$$\equiv \frac{K_a}{G_o} + \sum_p, \qquad [11]$$

where K_a is defined as the quantity in brackets and represents the sum of all fixed, cell and array costs per unit area. Eq. [11] shows that the cost/Watt contributions of all the power-related terms are independent

of the output power level. This is in contrast to the contributions from all other terms and results from the proportionality of the size of each power-handling element to the power level.

Now optimization of any single step m with respect to some variable of that step requires that the derivative of U with respect to that variable be zero. Because of the independence of the steps, only f_m and C_m are affected by such a variable. Therefore, when Eq. [11] is differentiated with respect to any variable of a cell step or an array step, $\sum_p$ remains fixed and does not contribute to the derivative. It is thus necessary to separate the optimization of all steps within K_a (all cell and array steps) from the rest.

Cell and Array Step Analysis

Separating out of Eq. [11] the properties of one step m from either the cell or array classes, we obtain

$$U = \frac{K'_{am} + C_m}{GF'_m f_m} + \sum_p = \frac{K'_{am}}{GF'_m}\left[\frac{1 + C_m/K'_{am}}{f_m}\right] + \sum_p$$

$$\equiv \frac{K'_{am}}{GF'_m}\left[\frac{1 + \kappa_m}{f_m}\right] + \sum_p \qquad [11a]$$

where $K'_{am} \equiv K_a - C_m$ and $\kappa_m \equiv C_m/K'_{am}$ can be regarded as a special type of cost fraction of step m relative to all the rest of the costs up to array completion (including fixed costs). Eq. [11a] displays a result of paramount importance: every step-efficiency factor until array completion has its same fractional impact on the cost/Watt of the entire array (although not on the subsequent power-handling elements). This is a direct consequence of the multiplicative roles of the f_j's in contrast to the additive contributions of the C_j's. In physical terms, this result says that any loss of power, regardless of its origin, decreases the value of the complete array in direct proportion; or alternatively, a proportionately larger (and proportionately more expensive) complete array would be needed to compensate the loss. Furthermore, Eq. [11a] shows that no step can be optimized by considering only its own cost and performance, since every expression for U to be minimized has in its κ_m the K'_{am} containing all the other costs.

To facilitate the optimization procedure we define for each step a fractional power *loss* $\lambda_j \equiv 1 - f_j$. Then the quantity to be minimized becomes

$$U = \frac{K'_{am}}{GF'_m}\left[\frac{1 + \kappa_m}{1 - \lambda_m}\right] + \sum_p, \qquad [12]$$

and, since the variables of step m are now exclusively in κ_m and λ_m, the quantity in brackets is all that need be minimized. Differentiating that quantity with respect to an appropriate variable of step m, which we denote by x, and setting the result equal to zero, we obtain the general optimization condition

$$\left[\frac{1}{1+\kappa_m}\right]\frac{d\kappa_m}{dx} = -\left[\frac{1}{1-\lambda_m}\right]\frac{d\lambda_m}{dx}. \qquad [13]$$

In many cases we find that $\kappa_m \ll 1$ (*i.e.*, $C_m \ll K'_{am}$) and $\lambda_m \ll 1$, so the optimization condition simplifies to the approximate relation

$$\frac{d\kappa_m}{dx} \simeq -\frac{d\lambda_m}{dx}. \qquad [14]$$

For these cases it is often convenient to rewrite the cost per Watt as

$$U \simeq \frac{K'_{am}}{F'_m G}[1+\kappa_m+\lambda_m] + \sum_p \simeq \frac{K_a}{FG}[1+\kappa_m+\lambda_m] + \sum_p, \qquad [15]$$

since $\kappa_m \ll 1$ is equivalent to $K'_{am} \simeq K_a$ and $\lambda_m \ll 1$ is equivalent to $F'_m \simeq F$. Thus, κ_m and λ_m are small perturbations on the approximate total array cost per output Watt, and optimization requires the minimization of the sum $(\kappa_m + \lambda_m)$ which we call the "penalty" for step m.

These relations have neglected cases for which Y_j may vary with a variable x. It has been shown by Smith Freeman of these Laboratories that in such cases, the effect is to add another similar term to $[1 + \kappa_m + \lambda_m]$ in Eq. [15].

Power-Handling Step Analysis

To deal with the power-related system elements most clearly, we revise Eq. [10] for K to express the power-related cost terms as they were given in Eqs. [6] and [7]

$$K = K_a + G_a \sum_{j=p}^{n} u_j f_p f_{p+1} \cdots f_{j-1} = K_a + G_a \sum_{j=p}^{n} u'_j \qquad [16]$$

where u'_j can be seen to be the cost/Watt of step j reduced by the product of the performance factors of the preceding power-related elements. This arises because the factor G_a, which is the full array power density, multiplies each term. It is significant that when step m being analysed is one of this class, only the terms of step m itself and those following it contain either u_m or f_m. The consequences of this are apparent when we express the cost/Watt as

$$U = \frac{K}{G_o} = \frac{K_a}{GF'_m f_m} + \frac{G_a}{GF'_m} \cdot \frac{1}{f_m} \sum_{j=p}^{n} u'_j. \qquad [17]$$

The factor $(1/f_m)$ multiplying the sum causes every term following the m term to lose its dependence on f_m and therefore drop out of the derivative of U (see Appendix). Thus only the array total and the *preceding* power-related terms influence the optimization of element m for the same reason that the power-related terms did not affect the optimization of an array step. Recalling the yield analogy for power in these elements, we can understand this result from the analogous general statement that yields affect all preceding steps only.

Defining now

$$U_{m-1} \equiv \frac{K_a}{G_a} + \sum_{j=p}^{m-1} u'_j \qquad [18]$$

as the total cost/Watt of everything preceding step m, it is shown in the Appendix that the condition for minimum U for any of these steps is precisely the same Eq. [13] found for the cell and array steps, provided that one changes the meaning of κ_m to

$$\kappa_m = \frac{u'_m}{U_{m-1}}. \qquad [19]$$

This then becomes the "cost fraction" to balance the power loss fraction λ_m for this class of system elements.

Discussion

Certain features of the results of this analysis are specific to the choice of formulation of the cost terms for the power-handling elements. Although the present choice seems most appropriate, an alternative might be justified in small systems. That would be to require that the power *rating* of all these elements be fixed at the same value, $G_a A_a$ so that $u'_j = u_j$ even though the evaluation of G_o would permit values of f_j less than unity. This would simplify the analysis and modify some of the conclusions, although the optimization Eqs. [13] and [14] would not change. The evaluation of κ_m would be the same for *all* steps of the system, given by $\kappa_m = C_m/K'_m$ where $K'_m \equiv K - C_m$. Moreover, every f_j would have its fractional impact on the cost/Watt of the full system.

In general, however, this analysis demonstrates that the cost-performance tradeoff for any step is accomplished quantitatively by placing on an equal footing the step's power-loss fraction and its "cost fraction", which must be evaluated as shown. The actual process of performing an

optimization requires, of course, sufficient information about a step so that the derivatives of Eqs. [13] or [14] can be evaluated. In the following paper[2] this procedure is used to obtain new optimum specifications for solar cell metallizations. We may note here that the cell efficiency η_c plays no role in the optimization, even for cell steps; it may be evaluated as a convenient milestone in reaching G_a using the relation

$$\eta_a = \eta_c \phi' \prod_{j=c+1}^{a} f_j.$$

The quantity ϕ' equals ϕ for flat-plate arrays, but for concentrator arrays ϕ' is the fraction of the array area that is made useful by the collector optics.

Of considerable importance in the optimization process is the imposition of any constraints that may be applicable to the variables of a step. We cite two prominent examples of such constraints:

(1) In the metallization on the front of a solar cell there are technological limits to the width and thickness of the metal lines that are applied. These must be invoked in formulating the expressions for $\kappa_m(x)$ and $\lambda_m(x)$ that are differentiated in Eqs. [13] or [14].

(2) The size of the energy storage facility in any system of this type is influenced by external factors such as the type of application of the system and the reliability desired of the energy supply. Not only does the coefficient u_m scale with the size of the storage facility (for fixed array size), but also the optimizations of the other steps may involve the storage costs.

It should be noted that, in the long run, the best criterion for optimization may be the minimum cost per Watt averaged over the life of the system rather than either the cost per peak Watt or cost per annual-average Watt. Such life-cycle cost determination will influence the cost terms in this procedure by the introduction of factors such as component lifetime and operating costs. As photovoltaic system development progresses and quantitative evaluation of those factors becomes possible, this type of optimization analysis should also evolve in this direction.

Finally, we note that this procedure need not be restricted in applicability to simple, flat-plate photovoltaic systems. Concentrator photovoltaic systems can be treated directly by the use in Eq. [7] of an appropriately small value of ϕ and the inclusion of array terms representing the optics, heat control, and tracking equipment. Tracking systems also increase the average value of G to be used in Eq. [2]. Furthermore, some other solar-electric generating systems are sufficiently similar in their classes of system elements that this analytic procedure should be quite directly adaptable to them also. This would seem to be the case for wind conversion systems and perhaps solar thermal electric generation sys-

tems. There appear to be analogous system components in solar building and hot water heaters, so that their cost and performance breakdowns should also be similar, provided one chooses a suitable analog to the power output of a photovoltaic system.

Appendix

For any power-related system element we show that the optimization condition is given by Eq. [13] derived for cell and array steps, provided that κ_m has the value given by Eq. [19]. The starting point here is Eq. [17] for U which we repeat

$$U = \frac{K_a}{GF'_m f_m} + \frac{G_a}{GF'_m} \cdot \frac{1}{f_m} \sum_{j=p}^{n} u'_j$$
$$= \frac{K_a}{GF'_m f_m} + \frac{G_a}{GF'_m} \left[\frac{1}{f_m} \sum_{j=p}^{m-1} u'_j + \frac{u'_m}{f_m} \right.$$
$$\left. + \sum_{j=m+1}^{n} u_j f_p f_{p+1} \cdots f_{m-1} f_{m+1} \cdots f_n \right]$$

which follows by simply grouping the steps from p to n. We show explicitly the cancellation of f_m from all terms following the mth step. We next form the derivative of U with respect to x, a variable of step m, and note that since only u_m and f_m are functions of x, the last group of terms do not contribute to the derivative. Setting the derivative equal to zero, we obtain

$$\frac{dU}{dx} = 0 = \frac{K_a}{GF'_m} \frac{d}{dx}\left(\frac{1}{f_m}\right) + \frac{G_a}{GF'_m} \left[\frac{d}{dx}\left(\frac{1}{f_m}\right) \sum_{j=p}^{m-1} u'_j \right.$$
$$\left. + \frac{d}{dx}\left(\frac{u'_m}{f_m}\right) \right]$$
$$= -\frac{K_a}{f_m^2} \frac{df_m}{dx} - \frac{G_a}{f_m^2} \frac{df_m}{dx} \sum_{j=p}^{m-1} u'_j + G_a \frac{f_m \frac{du'_m}{dx} - u'_m \frac{df_m}{dx}}{f_m^2}.$$

Removing the common factor $(1/f_m^2)$ and rearranging,

$$G_a f_m \frac{du'_m}{dx} = \frac{df_m}{dx} \left[K_a + G_a \left(u'_m + \sum_{j=p}^{m-1} u'_j \right) \right].$$

Dividing by G_a and using the definition for U_{m-1} in Eq. [18]

$$f_m \frac{du'_m}{dx} = \frac{df_m}{dx}\left[\frac{K_a}{G_a} + \sum_{j=p}^{m-1} u'_j + u'_m\right]$$

$$= \frac{df_m}{dx}\left[U_{m-1} + u'_m\right] = U_{m-1}\left[1 + u'_m/U_{m-1}\right]\frac{df_m}{dx}.$$

Now we label the fraction u'_m/U_{m-1} by κ_m for these elements as in Eq. [19] and obtain

$$f_m \frac{d\kappa_m}{dx} = \left[1 + \kappa_m\right]\frac{df_m}{dx},$$

$$\frac{1}{f_m}\frac{df_m}{dx} = -\left[\frac{1}{1-\lambda_m}\right]\frac{d\lambda_m}{dx} = \left[\frac{1}{1+\kappa_m}\right]\frac{d\kappa_m}{dx},$$

which is Eq. [13].

References:

[1] P. A. Crossley, G. T. Noel and M. Wolf, "Review and Evaluation of Past Solar Cell Development Efforts," Final Report to NASA by RCA Corp., Contract No. NASW-1427, June 1968. See Appendix II and references cited therein.

[2] D. Redfield, "Optimization of Solar Cell Contacts by System Cost per Watt Minimization," RCA Review, 38, p. 475, 1978 (this issue).

Optimization of Solar Cell Contacts by System Cost-Per-Watt Minimization*

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Abstract—New, and considerably altered, optimum dimensions for solar-cell metallization patterns are found using the recently developed procedure whose optimization criterion is the minimum cost-per-Watt effect on the entire photovoltaic system. It is also found that the optimum shadow fraction by the fine grid is independent of metal cost and resistivity as well as cell size. The optimum thickness of the fine grid metal depends on all these factors, and in familiar cases it should be appreciably greater than that found by less complete analyses. The optimum bus bar thickness is much greater than those generally used. The cost-per-Watt penalty due to the need for increased amounts of metal per unit area on larger cells is determined quantitatively and thereby provides a criterion for the minimum benefits that must be obtained in other process steps to make larger cells cost effective.

Introduction

Current efforts to apply photovoltaic energy conversion to terrestrial needs demand major reductions in the specific cost of the power generated. Such reductions require that an optimum be achieved in the tradeoffs between cost and performance at each step of the fabrication of a complete system. There is now available a general analytic procedure for achieving those optima[1] and this paper makes the first application

* This work was performed for the Jet Propulsion Laboratory, California Institute of Technology, under Contract No. 954352.

of that procedure to the analysis of the metal contacts of a solar cell. Although a variety of contact arrangements are in use, we apply this analysis here only to the most widely used contact arrangement on a circular silicon cell.

The difference between this and previous analyses is that this optimization is *not* restricted to minimizing the power loss, but rather, it minimizes the cost per watt U of the entire system as U is affected in both cost and performance by the metal contacts.

The analysis of the front contact is particularly useful for two reasons: (1) this has been one of the major expenses in previous cell fabrication processes and (2) there are four types of performance loss associated with the front contact and, although usually no one is very large, their sum is an appreciable fraction of the available power so that optimization of the patterns is very important.

Because, as will be seen, each of the terms expressing the fractional costs and fractional power losses is small compared to one, the optimization procedure of Ref. [1] is used in the simplified, approximate form appropriate for such cases. This requires minimization of the quantity called the penalty

$$P = (\kappa + \lambda). \qquad [1]$$

Here λ is the fractional power loss associated with the metallization and κ is the cost fraction of a metallization step relative to the complete array cost. In the terminology of Ref. [1], $\kappa = C/K_a$ where C is the cost of the metallization process per unit area of the array and K_a is the sum of the cost of the complete array plus the fixed costs of the system, all divided by the array area. Generally, it is necessary to include in C the yield factors of all subsequent steps and the fraction of the array covered by the cells. Independent estimates on real systems, however, show that by coincidence those two factors approximately cancel in the case of the metallization, so that C may be taken simply as the cost per unit *cell* area of the actual metallization step which in Ref. [1] was labeled k.

Eq. [1] for P neglects the possible effects of variations in the metallization process on the yield of that process; a third similar term would be required in the parentheses of Eq. [1] to account for yield variations.

As shown in Ref. [1], a minimum of P implies the optimization condition

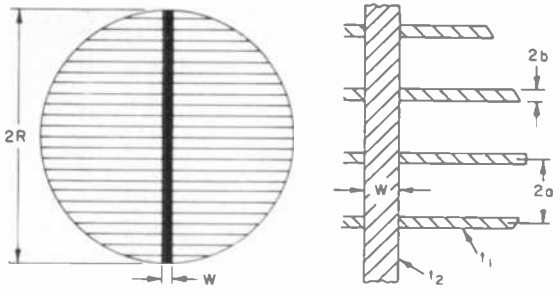
$$\frac{d\kappa}{dx} = -\frac{d\lambda}{dx} \qquad [2]$$

where x represents an appropriate variable of the step being analyzed;

in this case one such variable will be the metal thickness and another may be the metal line width or spacing of the fine lines.

Cell Model

To have a concrete example to optimize, we choose the most widely used cell and metal geometries—a circular wafer cell having radius R with metallizations consisting of a simple fine grid and a central bus bar from which the current is drawn at one end. This is shown in the upper part of Fig. 1, which also gives the other geometrical labels used for the fine



FRACTIONAL POWER LOSSES		
	FINE GRID	BUS BAR
SHADOW λ_S	b/a	$\frac{2W}{\pi R}$
RESISTIVE LOSS IN METAL λ_ℓ	$\frac{J}{V}\frac{\rho_m R^2}{4\lambda_S t_1}$	$2\ 24\frac{J}{V}\frac{\rho_m R^3}{W\ t_2}$
CONTACT LOSS λ_C	$\frac{J}{V}\frac{\rho_C}{\lambda_S}$	
SHEET RESISTANCE LOSS λ_{Si}	$\frac{J}{V}\frac{\rho_S}{\lambda_S^2}\frac{b^2}{3}$	

Fig. 1—Diagram of the cell and metallization geometries illustrating the symbols used here. The three specific resistances used are ρ_s ($\Omega/\square$) for the Si, ρ_c (Ω cm^2) for the Si-metal contact, and ρ_m (Ω cm) for the metal. Note $t_2 \neq t_1$.

grid and bus bar. The metal strips are equally spaced and all have parallel sides and uniform thicknesses, although the bus bar thickness t_2 may be different from that of the fine grid t_1. This would be appropriate for screen-printed metal contacts that appear to be most promising for these

applications; the fine grid and bus bar patterns would be applied separately to obtain different thicknesses.

It should be remarked that the parallel-sided bus bar is not the best possible choice. Having the new optimization criterion given by Eq. [2], it can be shown variationally that there exists an "ideal" shape (at fixed thickness) that gives a lower value for P than any other shape. This ideal shape has been determined by A. Moore for both circular and rectangular cells using constraints like those used here.[2] However, since the values of P for the bus bar are only a few percent lower using the ideal shape, we have retained the parallel-sided strip for simplicity.

The inclusion of appropriate physical constraints in the analysis is essential. For the fine grid pattern, the constraints used here are (a) the narrowest line that can be satisfactorily applied will be used and (b) the lengths of the lines are determined by cell borders as shown in the top left of Fig. 1. That the narrowest possible line should be used is well known and will be seen from the following analysis. The bus bar constraint is quite different. It can be shown formally and seen intuitively that the optimum bus bar geometry should be very narrow and thick, for any given amount of metal, to reduce the shadowed area of the cell. Therefore, we adopt the practical constraint that the width W must be four times the thickness t_2.

The remaining variables whose optimum values must be determined are the thickness t_1, the spacing $2a$ of the fine lines, and the thickness t_2 of the bus bar. Since b has been fixed, varying a is equivalent to varying the fine grid shadow fraction, $\lambda_{1S} \simeq b/a$. These variables will be used in place of the symbolic x in Eq. [2].

Evaluation of Cost and Performance Terms

Before Eq. [2] can be solved, the necessary dependences of κ and λ on the metal geometries must be determined. In keeping with the rest of the present treatment, we include only first order terms, leaving refinements for later calculation. For example, we write the cost per unit area of a metallization step as $C \simeq h + pv$ where v is the volume of metal used per unit area of the cell, p is the metal price per unit volume, and h represents the costs of machinery, labor and overhead that are allocated to a unit area of the cell. It is now assumed that h is independent of both the amount and pattern of the metal, so variations in the pattern geometries will appear only in v. Then in differentiating $\kappa = C/K_a$ for Eq. [2], the contribution h will always drop out. We thus redefine $C = pv$, retaining only the variable costs that will influence the optimization.

Now $v = v_c/A_c = ta_m/A_c$ where A_c is the cell area, v_c the volume of metal used on a cell, t is the metal thickness, and a_m the area of a cell covered by metal. In terms of the fraction of cell area shadowed by metal, $\lambda_S \equiv a_m/A_c$, we have $v = \lambda_S t$ so

$$C = p\lambda_S t \text{ and } \kappa = p\lambda_S t/K_a. \quad [3]$$

Note that $v = \lambda_S t$ is not explicitly dependent on either the cell size or the specific metal pattern.

Next we evaluate the fractional power loss terms to the same first-order level of accuracy. It is assumed that all the power loss terms of various types are simply additive and sufficiently small that the fractional power loss of each type is given by the quotient of the actual power loss and the cell generating capacity in the absence of any of the metallization losses. This approximation neglects the small decrease in available power as the current flows through successive stages of the device.

Another useful simplification stems from the constraints that are used. Since the lengths of the fine grid lines are fixed by the cell geometry and there is just a single central bus bar, there is no interaction between the properties of the fine grid and those of the bus bar. They are thus optimized independently.

The power loss terms are tabulated and evaluated in the lower part of Fig. 1. For the front bus bar there are two terms: the shadow loss

$$\lambda_{2S} = 2W/\pi R \quad [4]$$

and the resistive line loss given by

$$\lambda_{2\ell} = 2.24 \frac{J}{V} \frac{\rho_m R^3}{W t_2} \quad [5]$$

where ρ_m is the bulk resistivity of the metal (after heat treatment) and J and V are, respectively, the cell current density and voltage at the operating point. This last result is obtained by integrating the product of the square of the distributed current flowing into the bus bar and the resistance in a differential length, and then dividing by JA_cV, the cell's generating capacity.

A brief digression seems warranted at this point on the subject of equivalent series resistance associated with cell elements such as the bus bar (or other sources of dissipation). Such an effective resistance may be deduced from Eq. [5] by equating the actual power dissipation to I^2R_{eff} where $I = JA_c$ is the total cell current. It has been common practice, however, to compute an R_{eff} from a resistive voltage drop[3] or even just the geometrical resistance of a line $\rho_m\ \ell/A$.[4] In the present case of

a distributed source of current, however, these three methods of evaluating an R_{eff} give 3 different results and caution must be used in choosing the correct form for each application. We avoid the problem here by always calculating the power loss directly; no R_{eff} is used.

This optimization is now performed for a simple case that could not be optimized on the basis of performance alone, and one that provides a result of considerable further significance. We optimize the properties of a metal strip whose only loss is the resistive loss in the line λ_ℓ; since shadowing is excluded, this would apply to a bus bar of length $2R$ on the back of a cell. It is instructive here to replace W in Eq. [5] with the related quantity λ_S given by Eq. [4] so that

$$\lambda = \lambda_\ell = 1.43 \frac{J}{V} \frac{\rho_m R^2}{\lambda_S t}. \qquad [6]$$

The cost term has been shown to be given by Eq. [3] so $\kappa = p\lambda_S t/K_a$. Thus, the only two terms to be used in the optimization Eq. [2] contain the product $\lambda_S t = v$, but not either λ_S or t separately. This illustrates the point that neither λ_S nor t can be separately optimized in this case; only the product can. The proper variable to take the role of x in Eq. [2] is now $v = \lambda_S t$, and the optimization condition of Eq. [2] leads to

$$\lambda_S t = R \sqrt{1.43 \frac{J\rho_m K_a}{Vp}}. \qquad [7]$$

This optimum volume of metal per unit cell area may be arranged in any combination of thickness and width consistent with whatever constraints are applicable. Upon substituting this value for $\lambda_S t$ into Eqs. [3] and [6], we find that the cost fraction and loss fraction are equal

$$\kappa = \lambda = R \sqrt{1.43 \frac{J\rho_m p}{VK_a}}. \qquad [8]$$

The optimization procedure is applied next to the front bus bar and then the fine grid by finding the geometry for each that satisfies Eq. [2]. For the front bus bar, there are two sources of power loss as shown in Fig. 1: the line dissipation given by Eq. [5] and the shadowed area given by Eq. [4]. The cost term is still given by Eq. [3]. As noted earlier, it is necessary to introduce a physical constraining relating the metal width to thickness and we have chosen $W = 4t_2$ to give the thickest line that seems practical to apply. (Since the thickness of screen-printed metals shrinks to about half during heat treatment, the line is printed at a width/thickness ratio of 2.) Then $\lambda_{2S} = 2W/\pi R = 8t_2/\pi R$ and the only independent variable is t_2, in terms of which we now have

$$\kappa_2 = \frac{8pt_2^2}{\pi K_a R} \qquad [9]$$

and

$$\lambda_2 = \frac{8t_2}{\pi R} + 0.56\,\frac{J}{V}\,\frac{\rho_m R^3}{t_2^2}. \qquad [10]$$

Taking derivatives with respect to t_2 and making use of the optimization condition, Eq. [2], we obtain the equation for the optimum value of t_2

$$\frac{2p}{K_a}\,t_{2opt}^4 + t_{2opt}^3 - 0.44\,\frac{J}{V}\,\rho_m R^4 = 0, \qquad [11]$$

which must be solved numerically.

For an illustrative example we assume $K_a = \$0.0125/\text{cm}^2$, which corresponds to a (projected) array cost of 1\$/W, a 12.5% array efficiency, and 100 mW/cm^2 solar irradiance. We also assume cells made from 3-inch diameter wafers (so $R = 3.8$ cm), $J/V = 0.05\ \Omega^{-1}\ \text{cm}^{-2}$ (which corresponds to a fairly good cell whose performance is to be optimized over a full day, not just at solar noon), and for screen-printed silver contact metal $\rho_m = 3.2 \times 10^{-6}\ \Omega$-cm and $p = 1.30\$/\text{cm}^3$. These assumptions lead to $t_{2opt} \simeq 150\ \mu$m so $W = 0.6$ mm and $\lambda_{2S} = 0.01$. With these values, we find that $\kappa_2 = 0.016$ and $\lambda_2 = 0.031$, thus confirming the initial assumption that these fractions are much less than one. Nevertheless, the total penalty $(\kappa + \lambda) = 0.047$ shows that 4.7% of the array cost per Watt is attributable to this bus bar, although the actual cost of the metal is only 1.6% of the array cost. Thus the major part of the penalty is due to performance loss, not metal cost.

The fine grid pattern will be optimized next using the same procedure but with the constraints described earlier for this case. This case is more complicated than that of the bus bar because, as shown in the table of Fig. 1, there are four types of losses. In addition to the shadow and line loss that are present in the bus bar, we must include the resistive loss in the very thin front layer of the cell

$$\lambda_{Si} = \frac{J}{V}\,\frac{\rho_s b^2}{3\lambda_{1S}^2}, \qquad [12]$$

where ρ_S ($\Omega/\square$) is the sheet resistivity of the front layer, and the contact resistance loss at the metal-semiconductor interface

$$\lambda_c = \frac{J}{V}\,\frac{\rho_c}{\lambda_{1S}}. \qquad [13]$$

Here ρ_c (Ω-cm^2) is the specific contact resistance. Thus the full expression for the fractional power losses associated with the fine grid becomes

$$\lambda_1 = \lambda_{1S} + \frac{J}{V}\left[\frac{\rho_s b^2}{3\lambda_{1S}^2} + \frac{\rho_c}{\lambda_{1S}} + \frac{\rho_m R^2}{4\lambda_{1S} t_1}\right]. \qquad [14]$$

The numerical factor in the last term differs from that of Eq. [6] because it is computed by integrating the power loss over all the lines of different lengths.

In this case the minimization of the penalty requires the simultaneous optimization of both λ_{1S} and t (in contrast to the bus bar case for which that is not possible). This is best accomplished by partial differentiation of $(\kappa_1 + \lambda_1)$, first with respect to t_1 which, when set equal to zero, gives the first condition

$$v_{1opt} = \lambda_{1S} t_1 = R\sqrt{\frac{J\rho_m K_a}{4Vp}}, \qquad [15]$$

just as in Eq. [7] (except for the numerical factor). We thus understand this to be the optimization of the amount of metal per unit cell area. It also follows that

$$\kappa_1 \text{ (cost fraction)} = \text{line loss fraction} = R\sqrt{\frac{J\rho_m p}{4VK_a}}. \qquad [16]$$

These two terms of $(\kappa_1 + \lambda_1)$ are thus independent of λ_{1S} and t_1, so that partial differentiation of $(\kappa_1 + \lambda_1)$ with respect to λ_{1S} leads to the surprisingly simple equation for λ_{1S}

$$\lambda_{1S}^3 - \left(\frac{J}{V}\rho_c\right)\lambda_{1S} - \frac{2}{3}\frac{J}{V}\rho_s b^2 = 0. \qquad [17]$$

This is a noteworthy result in that the optimum shadow fraction is independent of cell size, metal cost and resistivity, and array cost. Those factors are significant only for determination of v_1; λ_{1S} then simply distributes the metal in the manner that optimizes the performance.

Moreover, in the familiar cases when ρ_c is small ($\lesssim 10^{-3}$ Ω-cm^2) enough to neglect the middle term

$$\lambda_{1S} \simeq \left(\frac{2J\rho_s b^2}{3V}\right)^{1/3}.$$

When this is substituted into the term for the sheet resistive loss in the front layer (i.e., that containing ρ_s), the value of that term becomes $\lambda_{1S}/2$. The only remaining term in $(\kappa_1 + \lambda_1)$ depending on λ_{1S} is the explicit shadow fraction itself. Thus we confirm that the smallest possible value of b should be used, as is the case when only performance is optimized.

Returning to the more general case in which λ_{1S} is found from Eq. [17] and v_{1opt} from Eq. [15], we evaluate the case used for the bus bar, i.e., the case of 3-inch diameter Si wafers, as a numerical illustration. We assume the Si front layer to have $\rho_s = 50\ \Omega/\square$, the specific contact resistance $\rho_c = 10^{-3}\ \Omega\text{-cm}^2$ and the minimum metal line width as $2b = 125\ \mu$m. These lead to a value of $\lambda_{1S} = 0.040$ (i.e., 4% of the area is covered by the fine grid metal). With the other values for the various parameters in Eq. [15], we obtain $t_{1opt} = 18\ \mu$m. Then $\kappa_1 = 0.008$ and $\lambda_1 = 0.069$. Thus the fine grid accounts for less than 1% of the actual expenditure but loses nearly 7% of the power (4% shadow and 2% Si resistance loss).

Combining now the optimized contributions of the fine grid and the bus bar

$$\lambda_{Tot} = \lambda_1 + \lambda_2 = 0.069 + 0.031 = 0.10$$
$$\kappa_{Tot} = \kappa_1 + \kappa_2 = 0.008 + 0.016 = 0.024 \qquad [18]$$

so the performance penalties far outweigh the cost contributions.

An illustration of the use of these results appears in Fig. 2 for 3-inch wafers with total array cost per Watt as the independent variable. It is important to note how the *total* cost influences the choice of metal parameter values. From the lowest curve, for example, it can be seen that for more expensive arrays it is worthwhile to increase greatly the amount of Ag to obtain a gain in performance.

Another use of these calculations is in connection with the question of how large the individual cells should be; this will become an important question as large-area sheets become available. Apart from any other considerations, it is clear qualitatively that as cell size increases, resistive losses in the metals will increase and the amount of Ag needed *per* cm^2 will increase. It is necessary therefore to determine quantitatively what impact those increases will have on U because they will have to be offset by potential benefits in handling fewer cells (e.g., fewer interconnections in the module). We have calculated the variation in optimum U as a function of cell size, using as reference a 1$/W array for 3-inch cells. The results shown in Fig. 3 indicate, for example, that an increase from 3-inches to 5-inches (12.7 cm) wafers requires that ~4% of U must be gained elsewhere in the fabrication to just compensate for the penalty

arising from the front metals alone. A significant consequence of this analysis was the conclusion from an extensive calculation[5] that *all* the anticipated processing benefits from handling fewer 5-inch cells would be cancelled by the penalty caused by the need for more metal, even at

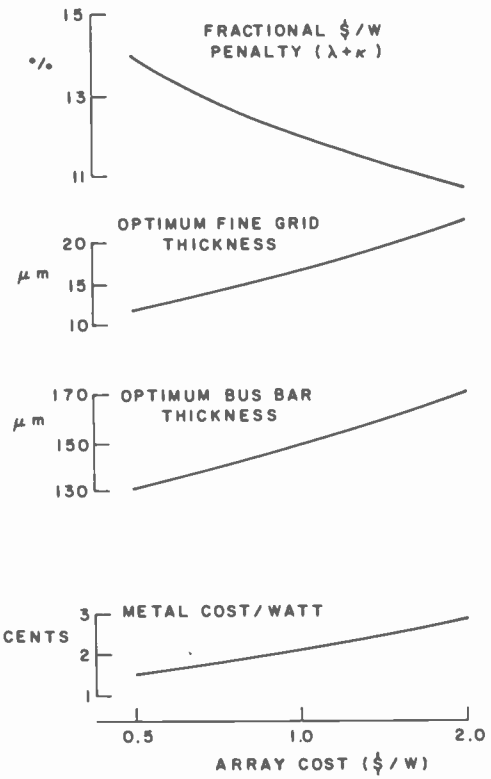


Fig. 2—Effect of total array cost in $/W (plotted logarithmically) on several front metallization parameters of 3-inch diameter cells with screen-printed Ag lines having straight, parallel sides. The curve ($\lambda + \kappa$) is obtained from totals like those in Eq. [18].

optimum conditions. That calculation, however, did not consider possible changes in the cost per unit area of the silicon sheet that might be associated with changes in wafer size.

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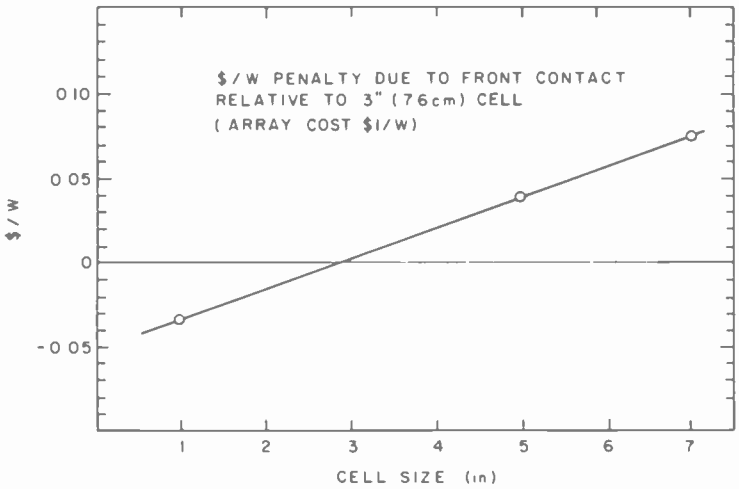

Fig. 3—Calculated penalty in $/W due to combined cost and performance contributions of optimum fine grid and bus bar on cell front as a function of cell size. The penalty is shown as a change from a reference array cost of 1$/W for all cell sizes with the zero arbitrarily set at the 3-inch (7.6 cm) wafer.

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Optimum Shape of the Bus Bar on Solar Cells of Arbitrary Shape

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Abstract—A complete procedure is given for determining the optimum shape of a central bus bar collecting current from a solar cell of circular or rectangular shape. It is applicable to cells of arbitrary shape. The method is a variational calculation that finds the form and adjusts the shape and thickness of the bus bar such that the cost, U ($/W), of the photovoltaic conversion system is a minimum. The bus-bar shape found for a given cell contour is the best possible shape for the given set of parameters. Assuming screen printed silver electrodes and array costs of $1/W, the cost reduction over a rectangular bus bar that has also been optimized for minimum system cost is small. However, the thickness is reduced by ~25%. Compared to a currently manufactured 3-inch diameter cell with an evaporated bus bar, the cost reduction is ~$0.072/W, a substantial amount. Also calculated is an optimum symmetrical bus bar that extracts the current through two leads, one at either end of the bus bar. For a 3-inch diameter cell, a cost saving over the optimum single-ended bus bar of $0.028/W and thickness reduction of ~33% is indicated, at the expense of interconnection complexity.

Introduction

Even though sunlight is free, if electric power generation by photovoltaic conversion is to become a viable alternative to conventional electric power sources, it is essential that the cost of the photovoltaic array be reduced to the absolute minimum possible within the capability of known or even projected technology. This is true regardless of the methods used to make the individual cells, whether single-crystal silicon, thin-film crystalline or amorphous material, or thick-film crystallites.

Every step in a projected process must be evaluated for its contribution to the net power output and the costs associated with that contribution. A general theoretical framework has already been constructed,[1] in which it is shown that the quantity to be minimized is total cost per watt of the system, U (\$/W), and that every step efficiency factor has its fractional impact on total cost per watt. It has also been shown[2] that while, generally, steps are interrelated and cost and performance must be considered for all steps simultaneously, the bus bar optimization becomes independent of the fine grid design for the front metallization step when the fine grid line length is determined. Many examples are given in Ref. [2] in which the dimensions of the screen-printed silver bus bars are optimized. The functional form of the bus bar, however, is assumed in that paper to be a single, central, uniform bar collecting current from the cell area.

In this paper, a very specific question is considered: given a cell of arbitrary but known shape, what is the optimum shape and thickness of a central bus bar such that its contribution to the total cost per watt shall be a minimum? By optimum shape we mean here the optimum width profile at optimum uniform thickness; thickness profiling is not considered, because it is thought to be technologically impractical. Attempts at an answer to the question can be seen in some commercial cells in which the bus bar is evaporated in the form of a wedge, narrow at one end and widening toward the lead contact where the total current in the bus bar is larger. We give here a systematic design method that yields the best possible shape for the given set of parameters. To make the method applicable to an arbitrary cell shape, the problem must be solved in its most general form. Important special cases are treated as appropriate.

Calculation

The calculation begins with the general economic equation given in Ref. [1], which is applicable to processes that have small cost increments or losses:

$$U_a = U_{ao}(1 + \kappa_m + \lambda_m). \qquad [1]$$

U_{ao} is the cost per watt of the collector array not counting the effect of the bus bar metallization step, κ_m is the fractional increase in cost arising directly from the metallization operation and λ_m is the fractional increase in cost indirectly attributable to the bus bar because of the loss of power output. κ_m is chosen to include only that portion of the cost of the process that scales directly with the amount of metal used, i.e., the cost of the

metal itself. This is because, seeking the minimum U_a, we will differentiate Eq. [1] with respect to a functional variable that would cause a constant term to disappear. λ_m is composed of two parts that contribute to power loss and hence to increased system cost per watt:

$$\lambda_m = F_{SH} + F_{LD}. \qquad [2]$$

F_{SH} is the shadowing fraction and F_{LD} is the fractional power loss in the resistive drop along the bus line.*

To calculate the three contributions to the cost increase we set up the geometry according to Fig. 1. Symmetry around the x-axis is assumed. $f(x)$ is the arbitrary but known shape of the periphery of the cell, $y =$

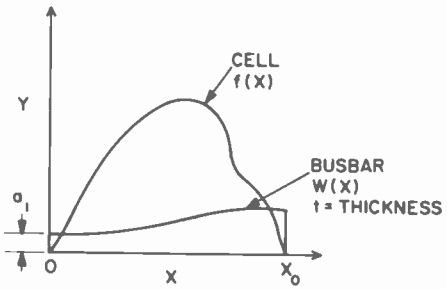

Fig. 1—Coordinate axes and geometry of the problem. The y-axis scale for $W(x)$ has been expanded for clarity.

$W(a_1,x)$ is the unknown shape of the bus bar where the half width at the narrow end, a_1, and the thicknesses t are to be determined.

F_{SH} can be written immediately:

$$F_{SH} = \int_0^{x_0} W(x)dx \Big/ \int_0^{x_0} f(x)dx \qquad [3]$$

F_{LD} is computed as follows. The total current in the full width bus bar at any point x is

$$I(x) = 2J_{mp} \int_0^x f(x')dx',$$

where J_{mp} is the photovoltaic current density at the operating point. From Ohm's law in the bar, the field $E(x)$ is related to the current density

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* This notation is different from that used in the previous paper, where F_{SH} is denoted λ_S and F_{LD} is λ_ℓ.

by the bus bar resistivity ρ_m:

$$E(x) = J(x)\rho_m = I(x)\rho_m/2W(x)t.$$

Since the field is also given by dV/dx, we have for the power dissipated in an increment dx of the bus bar

$$dP = I(x)dV = I^2(x)\rho_m dx/2W(x)t$$

$$= \frac{2J_{mp}{}^2\left[\int_0^x f(x')dx'\right]^2\rho_m dx}{W(x)t}.$$

Then

$$P = \frac{2J_{mp}{}^2\rho_m}{t}\int_0^{x_0}\frac{\left[\int_0^x f(x')dx'\right]^2 dx}{W(x)}$$

The fractional power loss is P/power output $= P/I_{mp}V_{mp}$ which leads to

$$F_{LD} = \left(\frac{b}{t}\right)\int_0^{x_0}\frac{\left[\int_0^x f(x')dx'\right]^2 dx}{W(x)} \Big/ \int_0^{x_0} f(x)dx, \qquad [4]$$

in which $b = J_{mp}\rho_m/V_{mp}$, a constant assumed known.

κ_m, the cost fraction of the silver, is given by the same formula as in Ref. [2],

$$\kappa_m = ptF_{SH}/K_a \qquad [5]$$

where p is the metal cost/cm^3 of metal in its final condition (i.e., after firing) and K_a is the cost/cm^2 of the array. When efficiency is specified, K_a can be related to U_a. The cost fraction κ_m and both loss fractions F_{SH} and F_{LD} are assumed small compared to one.

The problem now is to minimize Eq. [1] with respect to the *function* $y = W(x)$ or, what is the same thing, to find that function $W(x)$ that makes $\kappa_m + \lambda_m$ as small as possible and find that smallest value. In Ref. [2], in which the form of $W(x)$ was already assumed known (rectangular bus bar $W(x) = W/2$), it was shown that it is not possible to minimize U_a with respect to both metal thickness and shadow fraction because that leads to infinitely large t and zero W. An additional constraint was therefore imposed on the problem, namely that the thickness t always be 1/4 of the full line width W, a requirement compatible with screening technology. A similar constraint is required here. Since now $W(x)$ is not

a constant but increases with x, the constraint takes the form $W(x) \geq 2t$, which keeps the bus bar printable at its narrowest point, a_1. We now let

$$\int_0^x f(x')dx' = Z(x) \tag{6a}$$

$$\left.\begin{aligned} \frac{b}{t} \Big/ \int_0^{x_0} f(x)dx &= C_1 \qquad [6b] \\ \left[1 + \frac{p}{K_a} t\right] \Big/ \int_0^{x_0} f(x)dx &= C_2 \qquad [6c] \end{aligned}\right\} \text{independent of } x$$

In these terms, the mathematical problem is to minimize, with respect to the function $W(x)$, the sum

$$\kappa_m + \lambda_m = \int_0^{x_0} C_1 \frac{[Z(x)]^2}{W(x)} dx + \int_0^{x_0} C_2 W(x)dx, \tag{7}$$

subject to the constraint

$$W(x) \geq 2t. \tag{7a}$$

Problems of this sort are normally solved by the calculus of variations.[3] The special case of constraint with inequality conditions has been treated by Kuhn and Tucker.[4] The Lagrangian L is written in terms of the undetermined multiplier function $\lambda(x)$.

$$L = \kappa_m + \lambda_m - \int_0^{x_0} \lambda(x)[W(x) - 2t]dx.$$

Then the variational derivative $\delta L/\delta y = \partial L/\partial W(x)$ gives the Euler–Lagrange equation

$$\frac{-C_1[Z(x)]^2}{[W(x)]^2} + C_2 - \lambda(x) = 0. \tag{8}$$

Now either $W(x) > 2t$ and $\lambda(x) = 0$ or $W(x) = 2t$ and $\lambda(x) > 0$. Suppose $W(x) > 2t$ in a certain range of x. Then Eq. [8] gives

$$\frac{-C_1[Z(x)]^2}{[W(x)]^2} + C_2 = 0$$

or

$$W(x) = (C_1/C_2)^{1/2} Z(x). \tag{9}$$

Suppose $W(x) = 2t$ in another range of x. Then Eq. [8] no longer applies and the solution is simply

$$W(x) = 2t = a_1. \qquad [10]$$

Since $W(x)$ will be constant or monotonically increasing over all x from 0 to x_0, there will be a single dividing line or crossover point of x, below which Eq. [10] applies and above which Eq. [9] applies. Thus, Eq. [10] applies over the range $0 \leq x \leq a_2$ and Eq. [9] applies over the range $a_2 \leq x \leq x_0$. To find the crossover point a_2 (assuming the continuity of $W(x)$), set Eq. [9] equal to Eq. (10),

$$f_1(x) \equiv Z(x) - (C_2/C_1)^{1/2} a_1 = 0. \qquad [11]$$

The root of Eq. [11] gives a_2, and $W(x)$ is now completely defined. Substitution of $W(x)$ back into Eqs. [3], [4], and [5] using the definitions of Eq. [6], and minimizing the sum with respect to t or a_1 completes the problem.

It is not very helpful, however, to proceed beyond the present point before particularizing the problem to cell shapes of interest.
For a rectangular cell,

$$f(x) = a_b, \qquad 0 \leq x \leq x_0.$$

From Eq. [6a]

$$Z(x) = \int_0^x a_b dx' = a_b x$$

$W(x)$ is then of the form $W(x) = (C_1/C_2)^{1/2} a_b x$ for $a_2 \leq x \leq x_0$ (linear wedge) and $W(x) = a_1$ for $0 \leq x \leq a_2$.
For the circular disc,

$$f(x) = \sqrt{\left(\frac{x_0}{2}\right)^2 - \left[x - \left(\frac{x_0}{2}\right)\right]^2}.$$

From Eq. [6a]

$$Z(x) = \int_0^x f(x')dx' = \frac{1}{2}\left[\left(x - \frac{x_0}{2}\right)\sqrt{\left(\frac{x_0}{2}\right)^2 - \left(x - \frac{x_0}{2}\right)^2} + \left(\frac{x_0}{2}\right)^2 \left(\sin^{-1}\left(\frac{2x}{x_0} - 1\right) + \frac{\pi}{2}\right)\right].$$

$Z(x)$ is the cumulative area in the upper half plane of the disc swept out with increasing x. Eqs. [9] and [10] then define $W(x)$ as before. $W(x)$ is sketched for both cases in Fig. 2.

While it is, of course, possible to prove that $W(x)$ is the ideal form for the bus bar with the given set of parameters and constraint, it is not really necessary because of the nature of the variational solution. The Euler–Lagrange equation itself is derived by proving that it is a consequence

of the correct choice of the function whose integral is to be minimized.[3] On the other hand, there is nothing in the present solution that guarantees that a single central bus bar, even if optimized, will yield a lower loss fraction than some other geometrical configuration. At the present time, the only solution to that question is to guess a configuration, take

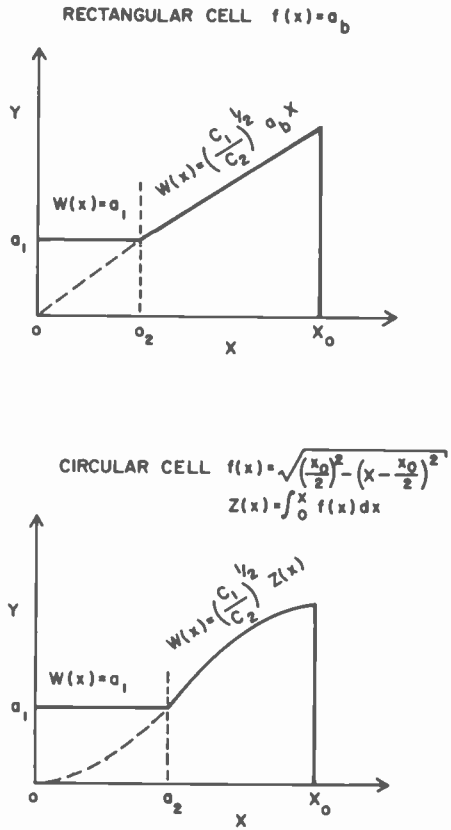

Fig. 2—Sketch of the variational solution for $W(x)$ for the two cases: rectangular and circular cells.

advantage of whatever symmetry is available, calculate the optimum loss fraction and bus bar shape by a scheme similar to the one presented here, and compare results. While not esthetically satisfying, such a trial and error approach will probably lead fairly quickly to a satisfactory design.

A complete solution useful in design of practical devices on cells of any shape must be obtained numerically. Because minimizing the cost of

Table 1—Optimum Bus Bar Using Optimum Function $W(x)$ for a Circular Cell: diameter x_0, area C, $J_{mp}\rho_m/V_{mp} = 1.6 \times 10^{-7}$; cost of silver p = \$1.30/cm^3 and bus bar resistivity $\rho_m = 2\rho_{Ag(bulk)}$ (screen printed); cost of array K_a = \$0.0125/cm^2 (\$1/W).

Dia. (inches)	3	5
x_0 (cm)	7.620	12.70
C (cm^2)	45.604	126.68
A_1 (cm)	0.0237	0.0378
A_2 (cm)	3.346	4.873
C_z (cm^{-2})	0.104	0.0447
F_{SH}	0.0114	0.0124
F_{LD}	0.0197	0.0305
λ_m	0.0311	0.0429
κ_m	0.0140	0.0244
$\kappa_m + \lambda_m$	0.0452	0.0674
t (μm)	119	189

Optimum function $W(x) = A_1$ for $0 \le x \le A_2$

$= A_1 C_z Z(x)$ for $A_2 \le x \le x_0$

where $Z(x) = \int_0^x f(x)dx$ and $f(x)$ is the cell periphery

solar cells is so important, the analysis has been carried out completely for the two cell shapes discussed above. The full procedure is given in the Appendix. The most important circular cell is given first, with typical results tabulated in Table 1 and a plot of the computed bus bar shape for a 3-inch cell in Fig. 3. Although for a circular cell the integrals can be evaluated analytically with some difficulty, numerical integration is used so that the same procedure is directly applicable to any cell shape merely by a suitable choice of $Z(x)$. The rectangular cell solution is given next with typical results in Table 2. This solution uses analytic evaluation of the integrals, which in this case is relatively simple.

Table 2—Optimum Bus Bar Using Optimum Function $W(x)$ for a Rectangular Cell: diameter x_0, area C, $J_{mp}\rho_m/V_{mp} = 1.6 \times 10^{-7}$; cost of silver p = \$1.30/cm^3 and bus bar resistivity $\rho_m = 2\rho_{Ag(bulk)}$ (screen printed); cost of array K_a = \$0.0125/cm^2 (\$1/W).

Length (inches)	3	5
x_0 (cm)	7.620	12.70
C (cm^2)	45.604	126.68
a_1 (cm)	0.0244	0.0391
a_2 (cm)	3.391	4.771
C_z (cm^{-2})	0.986	0.420
F_{SH}	0.0110	0.0119
F_{LD}	0.0194	0.0302
λ_m	0.0304	0.0421
κ_m	0.0139	0.0242
$\kappa_m + \lambda_m$	0.0443	0.0663
t (μm)	122	195

Optimum Function $W(x) = a_1$ for $0 \le x \le x_0$

$$= \frac{a_1 C C_z}{2}\left(\frac{x}{x_0}\right) \text{ for } a_2 \le x \le x_0$$

Table 3—Optimum Bus Bar Using Optimum Function $W(x)$ for a Circular Cell and Double-Ended Bus Bar (Two Leads): Diameter x_0, area C, $J_{mp}\rho_m/V_{mp} = 1.6 \times 10^{-7}$; cost of silver, bus-bar resistivity, and cost of array same as Tables 1 and 2.

Dia. (Inches)	3
$r = x_0/2$ (cm)	3.810
$C/2$ (cm^2)	22.8185
A_1 (cm)	0.01595
A_2 (cm)	1.583
C_z (cm^{-2})	0.208
F_{SH}	0.00530
F_{LD}	0.00705
λ_m	0.01235
κ_m	0.00440
$\kappa_m + \lambda_m$	0.0167
t (μm)	80

A third numerical example is also calculated in which the current is extracted from two leads, one at either end of the bus bar. The geometry is shown in Fig. 4. The cell is circular, the bus bar central, but symmetry about the y-axis is added. This case is easily derived from the single-

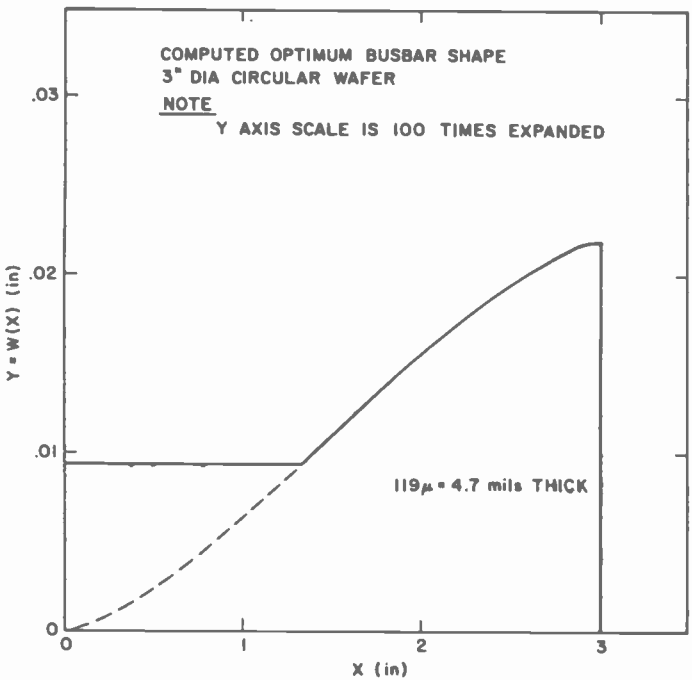

Fig. 3—Computed optimum bus bar shape for a 3-inch diameter circular wafer. Area = 45.60 cm^2, price of silver = \$1.30/cm^3, array cost = \$0.0125/cm^2 (\$1/W). Note that the y-axis scale has been expanded 100 times.

ended case by shifting the origin. Table 3 gives results for a 3-inch diameter cell. All three examples assume screen-printed silver bus bars on single crystal silicon cells.

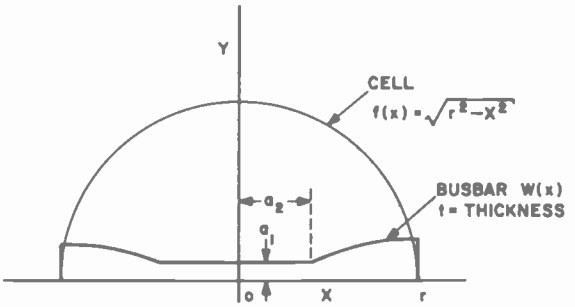

Fig. 4—Coordinate axis and geometry for a double ended bus bar, current extracted at both ends. The *y*-axis scale for $W(x)$ has been expanded for clarity.

Conclusions

A complete procedure has been given for determining the optimum shape of a central bus bar collecting current from a solar cell of circular or rectangular shape. The procedure is applicable to cells of arbitrary shape. The criterion is that the quantity U(\$/W) be a minimum. The savings to be realized by its use depend on to what the result is compared. For typical 3-inch and 5-inch diameter circular cells selling at a system cost of \$1/W, the total loss fraction $\kappa_m + \lambda_m = 0.045$ and 0.067 and the optimum bus bar thickness is 119 μm and 189 μm, respectively. The same cells with rectangular bus bars, also optimized for minimum \$/W, have loss fractions of 0.048 and 0.073 and optimum thickness of 153 μm and 261 μm, respectively. The saving due to the use of the ideal bus-bar shape is therefore small, \$0.003 and \$0.006/W, respectively. The 25% reduction in thickness would provide some slight technological advantage in shorter firing time and less danger of cracking and peeling. On the other hand, a 3-inch diameter circular cell of current manufacture using an evaporated silver rectangular bus bar shows a total loss fraction of 0.117. If this cell were in an array selling at \$1/W, the penalty for improper bus bar design would be \$0.072/W, a rather substantial amount inasmuch as we consider here only the bus bar and not the entire metallization. Since at present the cost far exceeds \$1/W, the penalty is actually that much larger. While, as noted above, the saving of optimum shape function over

optimum rectangular bar is small, it would appear that if one goes to the trouble of optimizing, one might as well go all the way and use the best possible procedure.

The double-ended bus bar shown in Fig. 4 achieves considerable saving over the corresponding single ended one. The total loss fraction for a double-ended optimized bus is 0.0167, yielding a saving of \$0.028/W at a system cost of \$1/W. The thickness is only two-thirds of the single-ended bus while the shadow fraction is only approximately one-half as much, meaning only one-third as much silver is required. The saving, of course, is purchased at the expense of increased complexity of the interconnections.

It should be noted that if minimum power loss is desired rather than minimum U, all formulas apply with the price of silver p set equal to 0. If technological or other limitations prevent the use of the optimum thickness and t must be considered fixed, the same formulas will yield the optimum shape under that limit. In that case, t being given, A_1 is immediately determined by $A_1 = 2t$. The solution proceeds from there.

Acknowledgments

I am greatly indebted to Smith Freeman for demonstrating to me the essential simplicity of a variational solution to the problem of minimization with constraints. I would also like to acknowledge the cooperation of David Redfield who devised the theroetical economic analysis referred to in the text and with whom I have worked closely on this and other problems.

Appendix—Numerical Solutions

Circular Cell, Diameter x_0, Area C

Let

$$\int_0^{x_0} f(x)dx = C/2 \text{ (1/2 cell area, assumed known)}$$

Main Program:

$$\text{Evaluate } F_{SH} = \frac{2a_1}{C}\,[a_2 + C_z I_2]$$

$$F_{LD} = \frac{4b}{Ca_1{}^2}[I_3 + I_2/C_z]$$

$$\kappa_m = \frac{pa_1}{2K_a} F_{SH}$$

$$\lambda_m = F_{SH} + F_{LD}, t = A_1/2$$

Evaluate: $\kappa_m + \lambda_m$ for a range of a_1 finding that value, A_1, that makes $\kappa_m + \lambda_m$ a minimum. Record $\kappa_m, F_{SH}, F_{LD}, \lambda_m, \kappa_m + \lambda_m, A_1, A_2, t$ for $a_1 = A_1$

$$W(x) = A_1 \qquad 0 \le x \le A_2$$
$$W(x) = A_1 C_z Z(x) \qquad A_2 \le x \le x_0$$

Subroutines:

rootfinder, function 1:

$$f_1(x) = Z(x) - 1/C_z = 0$$

root of $f_1(x) = 0$ gives a_2; $a_2 = A_2$ when $a_1 = A_1$.

numerical integration, function 2:

$$\int_{a_2}^{x_0} Z(x)dx = I_2$$

numerical integration, function 3:

$$\int_0^{a_2} [Z(x)]^2 dx = I_3$$

Evaluate C_z, function 4:

$$\left[\frac{2b}{\left(1 + \frac{pa_1}{2K_a}\right) a_1{}^3}\right]^{1/2} = C_z$$

Evaluate Z(x), function 5:

$$\left.\begin{aligned} \theta &= 2\cos^{-1}\left(1 - \frac{2x}{x_0}\right) \\ \frac{x_0{}^2}{16}(\theta - \sin\theta) &= Z(x) \end{aligned}\right\} \text{trigonometric form of } Z(x)$$

Rectangular Cell, Length x_0, Area C

Main Program:

Evaluate $F_{SH} = \frac{2a_1}{C}[F_1]$

$$F_{LD} = \frac{4b}{Ca_1^2}[F_2]$$

$$\kappa_m = \frac{pa_1}{2K_a} F_{SH}$$

$$\lambda_m = F_{SH} + F_{LD},\ t = a_1/2$$

Record κ_m, F_{SH}, F_{LD}, λ_m, $\kappa_m + \lambda_m$, a_1, a_2, t for the computed a_1

$$W(x) = a_1, \quad 0 \le x \le a_2$$

$$W(x) = \frac{a_1 CC_z}{2}\left(\frac{x}{x_0}\right), \quad a_2 \le x \le x_0$$

Subroutines:
rootfinder, function 5:

$$f_5(a_1) = \frac{p}{K_a} a_1^4 + a_1^3 - \frac{bC}{x_0}\frac{[F_2]}{[F_1]} = 0$$

root of $f_5(a_1) = 0$ gives a_1

Evaluate function 1:

$$\left[a_2 + \frac{CC_z}{4x_0}(x_0^2 - a_2^2)\right] = F_1$$

Evaluate function 2:

$$\left[\frac{Ca_2^3}{3x_0} + \frac{(x_0^2 - a_2^2)}{C_z}\right] = F_2$$

Evaluate C_z, function 4:

$$\left[\frac{2b}{a_1^3\left(1 + \frac{pa_1}{2K_a}\right)}\right]^{1/2} = C_z$$

Evaluate a_2, function 3:

$$\frac{2x_0}{CC_z} = a_2$$

Circular Cell, Diameter x_0, Area C with Symmetrical Bus Bar (Two Leads)

The only changes from the single-ended bus bar, circular cell, above are that we let

$$\int_0^r f(x)dx = C/4.$$

Wherever C appears in single ended case, write $C/2$. Wherever x_0 appears, write $x_0/2$ or r.

$Z(x)$ is now given by

$$\left.\begin{aligned} \theta &= 2\cos^{-1}(x/r) \\ \frac{r^2}{4}(\pi + \sin\theta - \theta) &= Z(x) \end{aligned}\right\} \text{trigonometric form of } Z(x)$$

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[1] D. Redfield, "Procedure for Minimizing the Cost Per Watt of Photovoltaic Systems," *RCA Review*, 38, p. 463, Dec. 1977 (this issue).

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[4] H. W. Kuhn and A. W. Tucker, "Nonlinear Programming," *Proc. Second Berkeley Symp. on Mathematical Statistics and Probability*, Univ. Calif. Press, Berkeley and Los Angeles (1951). See also a discussion of inequality conditions in *Economic Theory and Operation Analysis*, by W. J. Baumol, Prentice-Hall, Inc., Inglewood Cliffs, N.J. (1972), Third Edition, p. 151.

Silicon Epitaxial Growth via Dichlorosilane in a Barrel Reactor

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Abstract—This report presents the results of the study of silicon epitaxial growth using dichlorosilane in a large vertical barrel reactor. Thickness uniformity, surface quality, and resistivity control and uniformity of the epitaxial layers were studied and optimized in terms of the operating parameters of the system. Under the experimentally defined optimal conditions, thickness uniformity in the neighborhood of ±5% is achieved for growth rates in the range of 2 to 6 μm/min. The resistivity of undoped layers on heavily doped n^+ substrates is equal to or exceeds 100 ohm-cm. The doping control and resistivity uniformity are more than sufficient for growth of high-voltage device structures. Surface quality comparable to that obtained via silicon tetrachloride has been achieved.

I. Introduction

The epitaxial growth of silicon on silicon in a horizontal reactor[1–4] or vertical "pancake" reactor[2,3,5–7] and on sapphire[8] via dichlorosilane in hydrogen have been investigated and reported in recent years. Considerable interest in the subject was generated by the several attractive attributes of dichlorosilane as a source for silicon deposition. Another more important consideration is that the purity of commercially-available dichlorosilane already exceeds the most stringent requirement for an epitaxial silicon source material. Among the various desirable features, dichlorosilane is a liquid at room temperature but with a vapor pressure about 2 atm;[9] thus its introduction to the carrier-gas stream can be accurately controlled by gas flowmeters. It has also been reported that the

overall deposition rate is very nearly independent of temperature, thereby achieving improved control of both thickness and resistivity of the grown layers.[4] In addition, increased growth rate is obtained at appreciably lower growth temperature (1050 to 1100°C)[1,4,5] in comparison with silicon tetrachloride as a source.

This paper presents the results of a study of silicon epitaxial growth using dichlorosilane in a vertical barrel reactor. Thickness uniformity, surface quality, and resistivity control and uniformity of the epitaxial layers were studied and optimized in terms of the operating parameters of the system. Growth temperature, growth rate (concentration), flow velocity of carrier gas, substrate cleaning and in-situ etching or surface treatment procedures, choice of susceptor, substrate orientation, and air-cooling arrangement were among the various controllable operating parameters examined. Optimum conditions defined via these parameters are described and discussed in some detail.

2. Experimental

The epitaxial reactor used is a large industrial barrel reactor with a quartz bell jar measuring 7 inches in diameter, and 27 inches in height. It holds a silicon carbide coated graphite susceptor that has four tiers accommodating seven 2¼ inch silicon wafers, thus with a total capacity of 28 of these wafers. Another silicon carbide coated graphite preheater is placed on top of the seven-faced barrel susceptor. The susceptor is heated by rf induction at 450 KHz. The wall of the quartz reactor is cooled by air blown through two annular dispensers situated at the top and bottom of the bell jar. The flow control panel used was one with mass flowmeter controls for all the doping gases. The hydrogen carrier gas was carried via the common laboratory supply line and was derived from liquid hydrogen. Dichlorosilane (DCS, SiH_2Cl_2) was obtained from Linde Division of Union Carbide Corporation in 50 lb cylinder (#1 size) and was metered as a gas directly into the epitaxial reactor. Arsine and diborane in hydrogen at the 25 to 100 ppm level were used as the doping gases; they were further diluted with hydrogen in the manifold of the flow panel, and then injected into the reactant gas stream through the control of the mass flowmeter. Temperatures were measured using an optical pyrometer of the disappearing filament type and were not corrected for the emissivity of silicon or the absorption losses through the quartz wall of the bell jar and the quartz window of the reactor enclosure.

The silicon substrates used were for the most part antimony doped n^+ wafers at a resistivity of 0.01 to 0.015 ohm-cm and boron doped p^+

wafers at a resistivity near 0.01 ohm-cm. They were either 2 or 2¼ inch in diameter, oriented 1.5 to 3.0° off the (111) plane toward the nearest (110) or ±2° off the (100) plane. The wafers were all polished using colloidal silica and cleaned just prior to loading into the reactor. The silicon substrates usually were further cleaned by in situ HCl etching just prior to growth.[10]

The thickness of the epitaxial layers was determined using a Digilab Film Thickness Gauge FTG-12, and the resistivity by means of two point spreading resistance probe measurements. Thickness measurements of the epitaxial layers by reflective interference infrared spectroscopy using Beckman IR-5A and a cross-sectional spreading resistance probe were also made for comparison. Agreement of measured values on identical samples from the three different methods is excellent.

3. Growth Rates

3.1 Effect of Dichlorosilane Concentration, Growth Temperature, and Carrier Gas Flow

As reported earlier by Robinson and Goldsmith,[4] the growth rate is essentially the same over a temperature range of 30°C, which represents the maximum spread of the growth temperature among all the wafers in each run, as long as the temperature falls between 1030 to 1100°C (uncorrected). On the other hand, growth rate is approximately proportional to the concentration of dichlorosilane in the hydrogen gas stream and increases with increasing carrier gas flow for constant concentration of dichlorosilane. Fig. 1 shows the dependence of growth rate as a function of dichlorosilane concentration at several flow rates of hydrogen for a growth temperature of 1060°C (uncorrected).

3.2 Effect of Substrate Orientation

The (111) and (100) oriented single crystal wafers have been placed side by side in many runs, and no appreciable systematic differences in growth rate are observed between these two orientations.

4. Reactor Wall Deposit

4.1 Effect of Growth Parameters

The deposit on the wall of the quartz bell jar during the epitaxial growth cycle is found to be growth-rate insensitive and dependent only on the

total thickness of growth under controlled operating conditions. The deposit usually starts at the bottom of the bell jar at the position just below the susceptor and moves up, as growth proceeds, toward the top of the susceptor to a level determined by the thickness of the epitaxial layer grown. It is noted that the deposit pattern does not change with prolonged annealing of the substrate at the growth temperature just prior to growth. Given a certain growth rate, the carrier-gas flow and growth temperature do not seem to change the wall deposit appreciably, at least over the range studied.

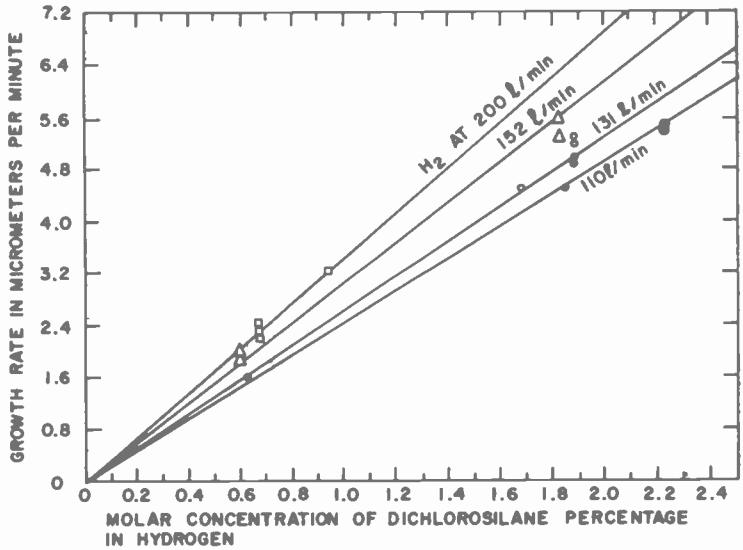

Fig. 1—Growth rate versus dichlorosilane concentration at various flow rates of hydrogen at 1050°C.

4.2 Influence of the Physical Set-Up for Gas Exhaust in the Reactor

An additional quartz heat shield placed above the existent heat shields, which are situated just below the susceptor, greatly increases the amount of deposit on the wall of the bell jar under otherwise identical operating conditions. Furthermore, if even one of the existing heat shields is replaced with one giving rise to a higher back pressure, the wall deposit increases too rapidly to allow the completion of thick epitaxial layer growth.

4.3 Minimization of Deposit on Reactor Wall

The amount of the deposit on the reactor wall is controlled to a very large extent by the cooling arrangement of the quartz bell jar during the growth. Insufficient cooling would inevitably lead to sparking between the rf coil and the wall deposit, thus necessitating the termination of the growth run. With the experimental arrangement described earlier and using only needed heat shields below the susceptor, the wall deposit can be reduced to the extent that no difficulty whatsoever was encountered for growth with thicknesses in excess of 150 μm. The rate of build-up of the wall deposit was approximately linear with time for the particular experimental arrangement. Furthermore, the wall deposit could be stripped away easily by means of in-situ HCl etching. The deposit on the reactor wall does not constitute a real handicap for the growth process.

5. Thickness Uniformity

5.1 Effect of Growth Rate and Growth Temperature

At a given flow velocity of the carrirer gas, the thickness uniformity of the epitaxial layers from tier to tier remains unchanged with growth rate in the range of 2 to 5.5 μm/min and growth temperature in the range of 1030 to 1100°C (uncorrected). The thickness variation is usually within ±5% of the mean among the wafers from the four tiers, with the ones from the first tier the thickest, the second tier the thinnest, and that from the third and fourth tier very close to the mean, provided the hydrogen flow is equal to or greater than a certain critical velocity, say 131 liters/min.

5.2 Influence of the Flow Rate of Carrier Gas

The influence of the flow rate of carrier gas on growth rate in the four tiers is given in Table 1. At a hydrogen flow rate of 110 liters/min, the growth rate decreases monotonically from the first to the fourth tier. For a hydrogen flow 131 liters/min or higher, the growth rate assumes the shape of a shallow dish from the first moving down to the fourth tier, i.e., higher at first and fourth tier and lower at second and third tier as compared to the mean. Furthermore, the thicknesses of epitaxial layers grown on wafers in the same tier have a much larger variation in the case of the 110 liters/min as compared to the 131 liters/min hydrogen flow, as shown in Table 2. Table 3 shows the thickness uniformity of the epi-

Table 1—Effect of Carrier-Gas Flow Rate on Growth Rate

Hydrogen Flow Rate, liters/min	Percentage of Dichlorosilane	Growth Rate, μm/min			
		Center, 1st Tier	Center, 2nd Tier	Center, 3rd Tier	Center, 4th Tier
110	0.62	1.82	1.76	1.64	1.56
131	0.67	2.13	2.06	2.19	2.26
152	0.60	2.12	1.90	1.90	1.95
200	0.64	2.49	2.14	2.20	2.40

Table 2—Effect of Carrier Gas Flow on Thickness Uniformity

Hydrogen Flow Rate, liters/min	Percent Dichlorosilane	Thickness of Epitaxial Layer, Center of 3rd Tier in μm						
		Wafer 1	Wafer 2	Wafer 3	Wafer 4	Wafer 5	Wafer 6	Wafer 7
110	0.62	74	76	80	82	82	81	78
131	0.67	99	99	99	100	100	100	100

taxial layer on individual wafers with regard to several locations on each of these wafers from each of the four tiers and for various flow rates of hydrogen (carrier gas). The variation in the thickness of the layers on each wafer and from tier to tier provides a very good measure of the thickness uniformity possible with the dichlorosilane process.

Table 3—Thickness of Epitaxial Layer as a Function of Location on Wafer

Growth Conditions	Tier	Thickness of Epitaxial Layer, μm				
		Center	Top	Bottom	Left Side	Right Side
Hydrogen 110 l/min Dichlorosilane 0.62%	1st	82	85	80	84	84
	2nd	79	80	78	81	79
	3rd	74	76	72	73	74
	4th	70	72	68	69	68
Hydrogen 131 l/min Dichlorosilane 0.67%	1st	96	104	93	99	97
	2nd	93	96	93	97	96
	3rd	99	100	98	103	100
	4th	102	104	97	102	99
Hydrogen 152 l/min Dichlorosilane 0.60%	1st	105	110	99	104	106
	2nd	93	96	93	96	97
	3rd	97	98	97	100	100
	4th	100	102	99	97	102
Hydrogen 200 l/min Dichlorosilane 0.69%	1st	116	123	109	118	119
	2nd	102	106	100	103	104
	3rd	106	106	107	109	110
	4th	118	118	118	120	117

6. Surface Quality

6.1 Substrate Cleaning

The surface quality of the epitaxial layers is primarily controlled by the effectiveness of the substrate cleaning. An inappropriate cleaning procedure brings about unacceptable results, but proper cleaning alone does not assure a desirable outcome if other procedures that follow are not done correctly. The critical importance of the cleaning step is considerably moderated, however, for the (100) oriented wafers as compared to the usually used (111) oriented ones in this study.

Two substrate cleaning schedules have been found to be satisfactory—one is the megasonic cleaning procedure and the other the standard scrubbing-acid cleaning schedule. The former involves ultrasonic cleaning in the megahertz range and the latter consists of vigorous scrubbing in a wafer scrubber followed by acid cleaning. Both procedures are effective only when the wafers are loaded into the epitaxial reactor immediately after they are cleaned.

6.2. In-situ HCl Etching Prior to Growth

In-situ HCl etching just prior to growth is also vital in obtaining a good surface quality of thick epitaxial layers. HCl concentrations of from 0.6 to 2% in hydrogen and etching times of from 5 to 10 minutes have been studied. The best combination (at an etch rate of approximately 1 μm/min) was found to be 1% HCl concentration and 10 minutes etching time.

6.3 Conditions of the Susceptor

It has been observed that a susception with a 25 to 30 μm silicon coating, deposited just prior to loading of the substrate wafers, consistently yields a better surface quality of the epitaxial layers than does a bare susceptor. Furthermore, the condition of the "preheater" part of the susceptor is of crucial importance to the surface quality. A physically integral preheater must be used in order to assure a desired surface quality of the finished wafers.

6.4 Wafer Orientation and Wafer Source

The (100) orienated wafer without a doubt has a better surface quality than the (111) oriented wafer grown under identical conditions and

cleaned via identical schedules. Identically oriented wafers from different vendors, i.e., from our in-house facility, Monsanto, SILTEC, Semi-elements, Wacker, and Semiconductor Specialities (Fairlawn, N.J.) all give comparable results when grown under similar conditions as far as surface quality is concerned, even though edge chipping is more serious in some than others.

6.5 Optimized Results

Under the optimal conditions described above, surface quality comparable to that obtained via silicon tetrachloride in all four tiers have been achieved.

7. Resistivity Control and Uniformity

7.1 Effect of Growth Rate

In the case of substrate wafers placed directly on the bare susceptor, the resistivity of the undoped epitaxial layer on a low resistivity substrate is dependent on growth rate via change in dichlorosilane concentration. For undoped layers grown on n^+ (111) wafers with a resistivity of 0.015 ohm-cm, the resistivity is 100 ohm-cm at a growth rate of 2.4 μm/min and 40 ohm-cm at a growth rate of 4.6 μm/min. This is consistent with what has been observed for growth in a horizontal reactor.[4] The general trend is that the higher the growth rate, the lower the resistivity of the undoped epitaxial layer on a heavily doped substrate.

7.2 Back-Sealing of the Substrate Wafer

As reported earlier, a 25 to 30 μm silicon coating on the susceptor is very desirable in improving the surface quality of thick epitaxial layers; moreover, it serves the purpose of back-sealing the substrate wafers. Most of the growth runs were made under this condition. The resistivity of the undoped epitaxial layers thus grown on heavily doped n^+ substrates shows a very weak (if any) dependence on the concentration of dichlorosilane in hydrogen, as the resistivity is invariably higher than 100 ohm-cm. Similarly, the variation in resistivity of layers from the first through the fourth tier is also minimized. Furthermore, use of a coated susceptor permits the growth of high resistivity opposite-type layers on heavily doped low resistivity substrate wafers with ease. For example,

Table 4—Distribution of Resistivity of Varous Epitaxial Layers for a pn^-np^+ Structure

	Substrate						
	p^+	n		n^-		p	
Tier	Resistivity ohm-cm	Resistivity ohm-cm	Thickness μm	Resistivity ohm-cm	Thickness μm	Resistivity ohm-cm	Thickness μm
1	0.01	0.4	28	34	71	0.65	42
2	0.01	0.5	25	54	67	0.62	41
3	0.01	0.46	26	65	69	0.64	40
4	0.01	0.46	26	65	75	0.68	41

0.5 ohm-cm n-type epitaxial layers can be routinely grown on 0.010 ohm-cm p^+ substrate wafers.

7.3 Dopant Control, Resistivity Uniformity as Applied to Growth of Device Structures

The resistivity of the various layers for the pn^-np^+ structure from first to fourth tier in a typical run is given in Table 4. The value of the resistivity is measured via spreading resistance probe and an actual tracing for one of the samples is shown as Fig. 2. Similarly, Table 5 gives data on the resistivity control of the epitaxial $\pi\nu/nn^+$ structure. A spreading resistance probe measurement for such a structure is shown in Fig. 3. The uniformity of resistivity for the epitaxial layers can be seen from the data presented in Table 6, where the resistivity value is measured as a function of location on the wafer for the four tiers of a growth run for a pn^-np^+ structure.

Table 5—Distribution of Resistivity of Various Epitaxial Layers for a $\pi\nu nn^+$ Structure

	Substrate								
	n^+	n		n		n^-		p^-	
Tier	Resistivity ohm-cm	Resistivity ohm-cm	Thickness μm	Resistivity ohm-cm	Thickness μm	Resistivity ohm-cm	Thickness μm	Resistivity ohm-cm	Thickness μm
1	0.015	2	9	9	31	30	30	31	37
2	0.015	2	10	9	29	39	29	34	32
3	0.015	2	9	12	30	52	29	33	34
4	0.015	2	9	13	28	50	28	38	34

Table 6—Resistivity Uniformity of Epitaxial Layers for a pn^-np^+ Structure as a Function of Location on the Wafer

	Tier	p^+ (Substrate) ohm-cm	n Resistivity ohm-cm	n^- Resistivity ohm-cm	p Resistivity ohm-cm
	Center	0.01	0.5	44	0.6
	Left	0.01	0.4	34	0.5
1	Right	0.01	0.3	28	0.5
	Top	0.01	0.4	27	0.5
	Bottom	0.01	0.4	29	0.5
	Center	0.01	0.5	50	0.6
	Left	0.01	0.3	25	0.5
2	Right	0.01	0.3	34	0.5
	Top	0.01	0.4	32	0.5
	Bottom	0.01	0.5	44	0.65
	Center	0.01	0.5	65	0.5
	Left	0.01	0.4	44	0.5
3	Right	0.01	0.5	80	0.6
	Top	0.01	0.4	70	0.45
	Bottom	0.01	0.4	80	0.6
	Center	0.01	0.44	60	0.6
	Left	0.01	0.42	30	0.7
4	Right	0.01	0.4	60	0.6
	Top	0.01	0.4	>100	0.54
	Bottom	0.01	0.4	40	0.7

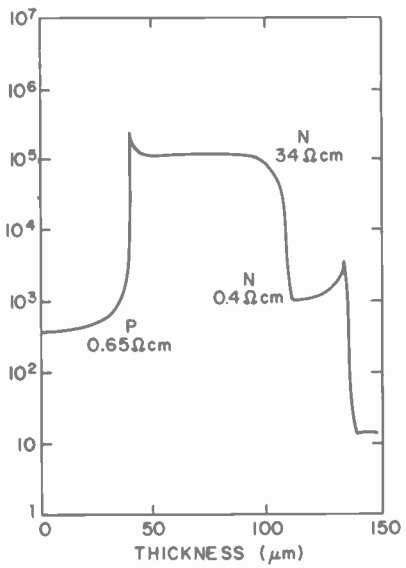

Fig. 2—Resistivity of epitaxial layers versus distance from substrate interface from spreading resistance measurements of a high voltage pn^-np^+ structure.

8. Discussion

Based on the data presented in Fig. 1, the growth rate per unit input of dichlorosilane at constant molar concentration, but different flow rates of carrier gas, can be calculated. It remains essentially the same for flow rates of 110 to 152 liters/min hydrogen, then declines appreciably per unit input of dichlorosilane for 200 liters/min. This relatively constant

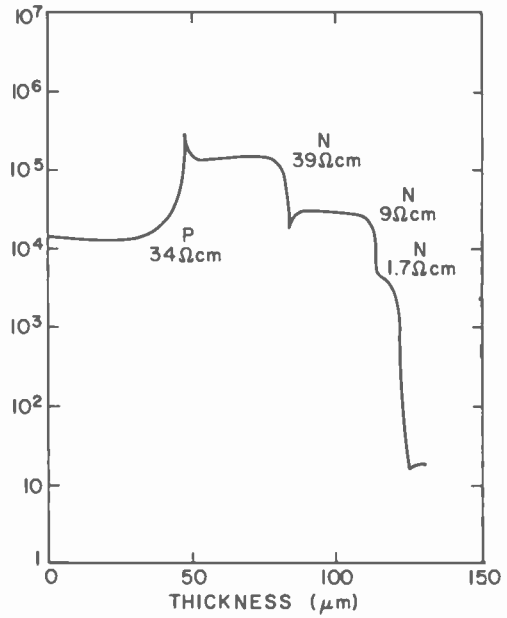

Fig. 3—Resistivity of epitaxial layers versus distance from substrate interface from spreading resistance measurements of a $\pi\ \nu nn^+$ structure.

chemical conversion efficiency coupled with the linear dependence of growth rate on mole fraction of dichlorosilane in hydrogen establishes the desired operating range of carrier gas flow. Furthermore, it accounts for the experimental observation that the deposit on the reactor wall is insensitive to growth rate and dependent only on the total thickness of growth as reported earlier.

The observed thickness uniformity of the epitaxial layers from the four tiers (as influenced by growth temperature, mole concentration of dichlorosilane, and flow rate of carrier gas) is consistent with the model proposed by Eversteyn[11,12] for growth rate versus position along the susceptor at different gas velocities of a tilted susceptor in horizontal

reactors. Surface quality of the thick epitaxial layers is maintained only with total absence of dust particles as well as carbon or oxide contaminants on the wafer surface prior to growth. As a result, the substrate wafers must be loaded immediately after cleaning, a nondefective preheater and susceptor must be used, and in-situ HCl etching at elevated temperature just prior to growth is required.

The dependence of the resistivity of undoped layers for nonbacksealed n^+ substrate wafers on the rate of growth is probably caused by the power dependence on the HCl concentration of the autodoping process and the linear dependence of epitaxial silicon growth rate with molar concentration of dichlorosilane in hydrogen. A power dependence of the order of 3 for the vapor transport of antimony via HCl (the accompanying pyrolysis product of dichlorosilane) is quite likely from the chemical-reaction point of view. A silicon layer 25 μm or thicker used to backseal the n^+ substrate wafer served as a sufficient diffusion barrier to prevent any significant autodoping effect.

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A 25-kV Bias-Isolation Unit for 1-MHz Capacitance and Conductance Measurements*

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Abstract—The measurement of small signal (differential) capacitance (C) and conductance (G) at 1 MHz as a function of applied-bias voltage can be carried out with a commercially available capacitance/conductance (C/G) meter at moderate applied-bias voltage ($\lesssim 100$ V). However, C and G measurements of metal-sapphire-silicon capacitors for characterizing silicon-on-sapphire require the use of much larger applied-bias voltage.

This paper describes a technique for using a commercially available C/G-meter with a Bias-Isolation Unit (BIU) for C and G measurements at bias-voltage magnitudes up to 25 kV without damage to the measurement equipment. The basic principles of operation and the details of the electrical design of a BIU are presented.

The use of the BIU imposes certain limitations on the range of sample capacitance and conductance that may be measured without introducing excessive error. The theory of these limitations is presented and compared with experimental results obtained from the use of the BIU. The measurement capability demonstrated by these results is adequate for the intended silicon-on-sapphire measurement application and may be described in terms of a measurement range for a maximum *added error* due to the use of the BIU. For less than $\pm 1\%$ added error in the indicated (measured) capacitance, the measurable range of sample capacitance is found to be from 0 to about 100 pF. In this application, it is also important to be able to accurately measure small changes in the sample capacitance; for less than $\pm 1\%$ added error in the indicated (measured) value of a small change in the sample capacitance, the measurable range of the sam-

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ple capacitance is found to be from 0 to about 38 pF. Conductance measurements may be made with less than about 2% added error for samples whose capacitance is in the range 0 to 50 pF.

1. Introduction

A technique for using a commercial 1-MHz capacitance meter (C-meter) for measurements at bias-voltage magnitudes up to 10 kV without risk of damage to the measurement equipment has been described in a recent report.[1] The technique involves the use of a Bias-Isolation Unit (BIU) that allows the bias voltage to be applied to the sample, but not to the C-meter. In addition, the BIU isolates the bias-voltage supply from the high-frequency test signal and permits the capacitance measurement to be made without excessive error. A BIU of this type has been used to carry out "modified" or extended-range MIS $C(V)$ measurements[2] of Al-sapphire-Si capacitors fabricated from silicon-on-sapphire (SOS).[3] It was shown that such measurements can be used to characterize SOS and the Si–sapphire interface[3] as well as to determine the effects of oxidation and hydrogen annealing[4] and exposure to soft X-rays[5] on the Si-sapphire interface.

In all of this work the sapphire substrates for the SOS were lapped and polished to final thickness in the range 125 to 190 μm. Although the ± 10 kV bias capability was sufficient for characterization of Si on these sapphire substrates, it was clear that a larger bias capability would be required if thicker substrates were to be used. Since 2 inch-diameter substrates used for production of integrated circuits on SOS are typically 250 and 325 μm in thickness and since it was anticipated that larger diameter substrates ranging up to $\sim$400 μm in thickness would eventually be used, it was decided that a new BIU with a larger bias-voltage capability should be developed. It is desirable to be able to use these thicker sapphire wafers to characterize the Si-sapphire interface, since this would allow the characterization of the same wafer on which the devices are being fabricated or, alternatively, identical starting wafers as monitors during device processing. Thus, a primary objective of the present work was the extension of the previously developed capacitance measurement capability to bias-voltage levels up to ± 25 kV for characterization of SOS.

The extended-range capacitance measurements can be used to determine the Si–sapphire interface-state density[3] using point-by-point differentiation of an experimentally derived quantity.[6] It has been shown that $G(V)$ measurements (ac conductance measurements as a function

of voltage) are capable of providing information about the $Si\text{-}SiO_2$ interface-state density,[7,8] but this type of measurement had never been carried out on SOS, nor was it clearly feasible. Certainly, no instrumental capability for it existed. Accordingly, a secondary goal of the present work was to provide an instrumental capability for implementing and evaluating MIS $G(V)$ measurements on SOS.

It is important to point out that while the accuracy requirements for the MIS $C(V)$ measurements are quite stringent, since the data (or a quantity derived from the data) must be differentiated to obtain the desired density of states information, the $G(V)$ data is used directly. Thus, although an error limit of about ±1% on $C(V)$ measurement is sought, an error of ±5 to 10% on $G(V)$ is reasonable for the measurement purpose intended.

There is at the present time only one commercially available 1-MHz C-meter that can also function as a conductance meter (G-meter)—the PAR Model 410.* A modified version of the instrument was obtained for the work described here. These modifications were:

(1) a 10× increase in the test signal level to produce a similar increase in the signal-to-noise ratio of the analog output signal, $\Delta C(V)$ and
(2) extra filtering to eliminate the effect of harmonics in the test signal. This point is discussed in some detail in Ref. [1].

In Sec. 2, the BIU circuit is considered from the point of view of both a functional description and the effect of the circuit on measurement accuracy. Some experimental results obtained using the BIU are presented in Sec. 3. An example of a typical measurement application is presented in Sec. 4. Finally, Sec. 5 contains some further discussion and conclusions.

2. Circuit

2.1 Functional Description

A schematic circuit diagram of the C/G-meter BIU is shown in Fig. 1, and the individual circuit elements are described in Table 1.

Fig. 2a is a front view of the BIU and the connections to it are shown schematically in Fig. 2b. The HI side of the TEST and DIFF terminals of the BIU are connected together and to the C-meter terminal marked INPUT. The LO side of the TEST and DIFF terminals of the BIU are

* PAR (Princeton Applied Research Corp.) Model 410 CV Plotter. In the present work, only the C/G-meter portion of the instrument is used.

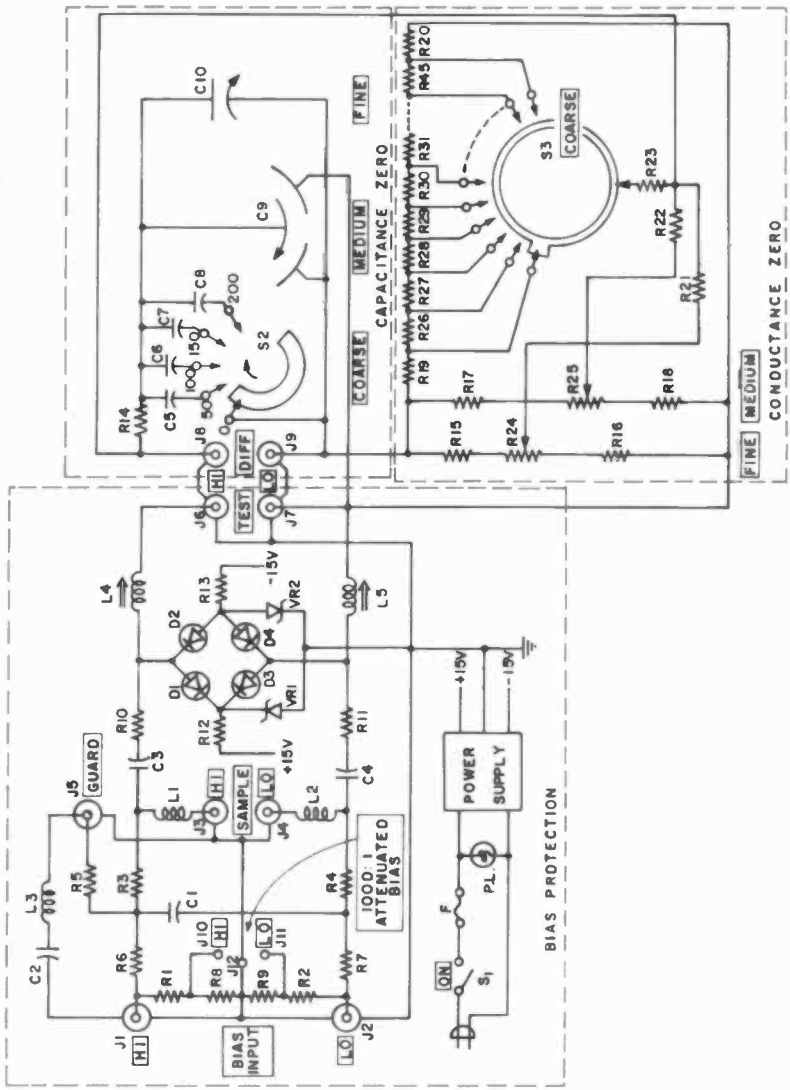
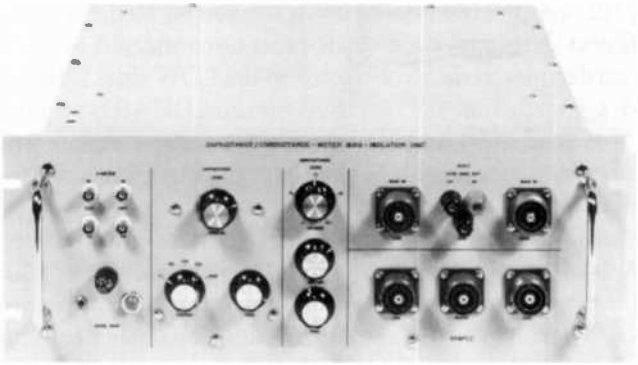


Fig. 1—Schematic circuit diagram of C/G-meter bias-isolation unit (BIU).

Table 1—Electrical Parts List for C/G-Meter Bias-Isolation Unit (See Fig. 1)

Schematic Reference	Description (Commercial designation* if appropriate shown in parentheses)
R1,R2,R3,R4,R5	$5 \times 10^4\ \Omega$, 1%, 12.5 W (Victoreen MOX 5)
R6,R7	$5 \times 10^5\ \Omega$, 10%, 2W
R8, R9	Use two resistors in series or parallel to obtain 1000:1 attenuation with $10^4\ \Omega$ load between J10 and J11
R10,R11	Series string of 50 1-Ω @ 3 W, noninductive resistors
R12,R13	820 Ω, 10%, 2 W
R14	100 Ω, 1%, 2 W
R15,R16	$20 \times 10^3\ \Omega$, 5%, 2 W, noninductive
R17, R18, R19, R20	$5.1 \times 10^3\ \Omega$, 5%, 2 W, noninductive
R21	$10^4\ \Omega$, 5%, 2 W
R22	$20 \times 10^3\ \Omega$, 5%, 2 W, noninductive
R23	500 Ω, 5%, 2 W, noninductive
R24,R25	10 turn, vernier adjustable carbon potentiometer $10^4\ \Omega$, linear taper
R26-R45	510 Ω, 5%, 1/2 W
C1,C2,C3,C4	0.001 μF @ 50 kVDCW (Plastic Capacitors OFN500-102, Extended Foil)
C5,C6,C7,C8	51 pF Silvered Mica @ 500 V
C9	33-0-33 pF differential type variable capacitor with speed-reducing planetary drive (E.F. Johnson Type "L" No. 167-0033-001) (Jackson Brothers Type 4511/DAF planetary ball drive with 6:1 ratio)
C10	2.2-10 pF variable capacitor with speed-reducing planetary drive (E. F. Johnson Type "L" No. 167-0001-001) (Jackson Brothers Type 4511/DRF dual ratio (36:1 and 6:1) planetary ball drive)
D1,D2,D3,D4	Type 1N482A diode
L1,L2	Special choke, 58 turns wound on C3 and C4
L3	Special choke, 90 turns wound on C2
L4,L5	3-5.5 μH adjustable (North Hills type 120B)
J1,J2,J3,J4,J5	High-voltage coaxial chassis connector (Amphenol type 97-3102A-18-420S)
J6,J7,J8,J9	Insulated BNC coaxial chassis connector (Amphenol type 31-010)
J10,J11,J12	Insulated banana jack
S1	SPST toggle switch
S2	Ceramic insulated continuous shorting-type switch (Centralab type PA-300 shaft and index assembly with type PA-13 ceramic switch section)
VR1	Type IN3305B Zener diode
VR2	Type IN3305RB Zener diode
Fuse	Type 3AG-1A
Power Supply	Regulated with + and −15 V outputs (Semiconductor Circuits Type 2.15.100)
S3	Ceramic insulated 21-position shorting-type switch (Centralab Type PA4002)

*Designation of commercial components in this table and elsewhere in this paper does not imply recommendation or endorsement of these components, nor does it imply that they are necessarily the best available for the purpose.



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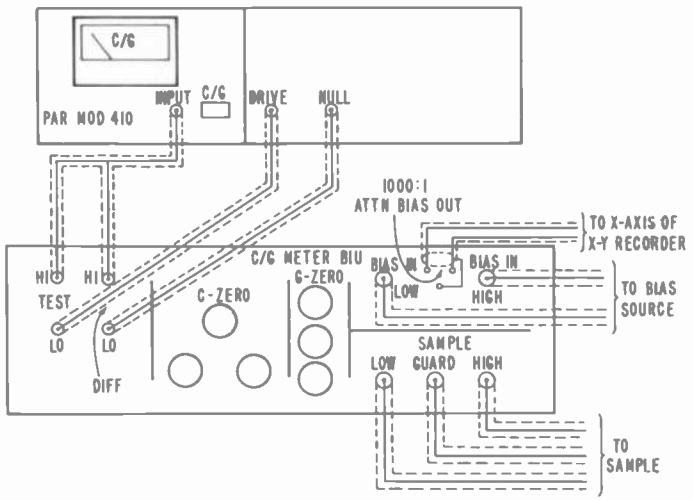

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Fig. 2—(a) Front view of C/G-meter BIU and (b) schematic drawing of connection to C/G-meter BIU.

connected, respectively, to the C-meter terminals marked DRIVE and NULL.

The capacitor to be measured is connected to the terminals marked SAMPLE, and the bias-voltage power supply is connected to the terminals marked BIAS INPUT. If a guard-ring-electrode system is to be used on the sample, the guard ring is connected to the terminal marked GUARD and the guarded electrode must be connected to the HIGH side; the unguarded electrode is connected to the LOW side. If the sample does not have a guard ring, the terminal marked GUARD should be terminated ("blanked off") with an insulated, unwired mating connector to prevent surface breakdown or "arcing" during high-voltage operation of the BIU.

The terminals marked 1000:1 ATTN BIAS should be connected to the X-Axis of an X-Y recorder with an input resistance of 10^6 ohms for a directly calibrated measure of the bias applied to the sample.

The BIU performs three major functions: (a) bias protection; (b) capacitance-zero adjustment; and (c) conductance-zero adjustment. The portions of the circuit which perform these functions are indicated in Fig. 1, and described below.

(a) Bias-Protection Circuit*

The high and low terminals of the output of the C-meter are individually clamped by diodes (D1 and D2 on the high side, D3 and D4 on the low side) to remain within some allowable range with respect to ground. Each of the diodes D1 through D4 has low-forward resistance, high-reverse resistance, and fast turn-on. To reduce their loading effect on the C-meter, they are normally maintained at a reverse bias of 6.8 V. The bias voltages (+6.8 and −6.8 V) are provided with a very low source impedance by the Zener diodes, VR1 and VR2.

The high-voltage blocking capacitors C3 and C4 are at (or nearly at) series resonance at 1 MHz with L1 + L4 and L2 + L5, respectively. Adjustment of L4 and L5 can be used to compensate for series inductance of the connecting leads both inside and outside the BIU.

High-frequency noise from the bias supply is attenuated by the low-pass filter formed by R6, R7, and C1. The resistors R3 and R4 and the capacitor C1 form a filter isolating the bias supply from the 1-MHz measurement signal.

A bias voltage equal to that at the high side of the sample is available at J5 for application to a guard-ring electrode. The 1-MHz series reso-

* A more detailed description of the bias-protection function is given in ref [1].

nant circuit formed by L3 and C2 assures that the guard ring is effectively grounded at the measurement signal frequency.

This portion of the circuit also contains a voltage divider, formed by R1 and R8 on the HIGH side and R2 and R9 on the LOW side, that serves to attenuate the bias input so that it may be fed directly to the X-axis of an X-Y recorder. The voltage divider is arranged so that if the input resistance of the recorder is 10^6 ohms, the bias attenuation factor will be 1000:1. If a recorder with a different input resistance were used, an appropriate correction factor could be calculated from the values of R1, R2, R8, R9, and the input resistance.

(b) C/G-Meter Operation

The operation of the C/G-meter in combination with the BIU is most easily understood by referring to the simplified equivalent circuit shown in Fig. 3.

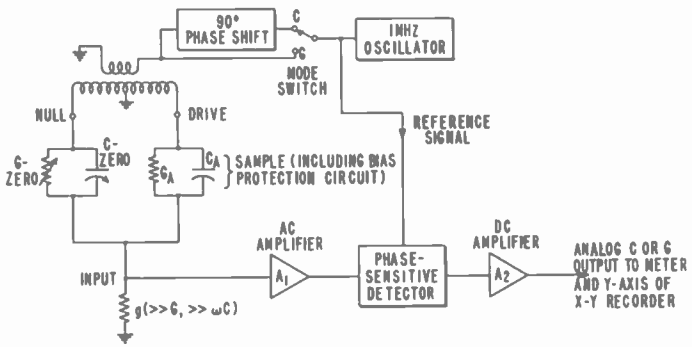

Fig. 3—Simplified equivalent circuit of C/G meter and BIU.

Consider first the operation when C-Zero and G-Zero are "zero," i.e., they are effectively removed from the circuit. A 1-MHz oscillator provides a modulation or drive signal to the sample under test as well as a reference signal to the phase sensitive detector (PSD). The sample as shown in Fig. 3 includes the bias protection circuit, the effect of which will be considered in Sec. 2.2. The current that flows through the sample in response to the drive voltage is converted to a voltage by the conductance, g, which is very large in comparison with both the sample susceptance and conductance. The voltage developed across g is amplified by A_1 and synchronously demodulated with respect to the reference signal by the PSD, thereby producing a quasi-dc level (propor-

tional to C or G) that is further amplified by A_2 to produce the signal labeled OUTPUT. If the mode switch is in position G, the PSD will "recognize" only that component of the input signal that is *in phase* with the reference signal. For a fixed magnitude of drive voltage, the output will be proportional to the conductance G_A of the sample. Similarly, if the mode switch is in position C, the PSD will recognize only that component of the input signal which is *in quadrature* with the reference signal. In this case, for a fixed magnitude of drive voltage, the output will be proportional to the sample capacitance C_A. The output is used to feed both a panel meter and an X-Y recorder, each of which is calibrated to read directly in the appropriate units of C or G.

The discussion thus far has assumed that C-ZERO and G-ZERO are removed from the circuit. We now consider the effect of including those circuit elements in Fig. 3. The voltage at the terminal marked NULL is equal in magnitude to that at the DRIVE terminal but is 180 deg out of phase with it. The currents through C-ZERO and G-ZERO can be used to null or cancel those through C and G of the sample, thereby allowing zero correction or zero adjustment of both C and G. This is useful not only for the usual nulling of stray capacitance due to the sample holder and connecting leads, but also for operation in a suppressed-zero mode, as is required for modified or extended-range MIS $C(V)$ measurements[2–6] and for the MIS $G(V)$ measurements discussed in Sec. 1. The actual capacitance-zero and conductance-zero circuits shown in Fig. 1 are somewhat more complicated than their simplified equivalents in Fig. 3; they are discussed in more detail below.

(c) Capacitance-Zero Circuit

Both large range and excellent precision of the CAPACITANCE-ZERO function are obtained by using three stages of adjustment, appropriately labeled COARSE, MEDIUM, and FINE. The COARSE and FINE stages (C5-8 and C10 in Fig. 1) provide a variable capacitance between the NULL and INPUT terminals. The medium stage of CAPACITANCE-ZERO adjustment (C9) is a capacitive divider between the DRIVE and NULL voltages (see Fig. 2b), capable of canceling out the minimum value of C10 plus the stray capacitance of the wiring, thereby allowing the total capacitance-zero correction or adjustment range to include "zero," i.e., *no correction*.

The total range of capacitance-zero correction is approximately 250 pF. To facilitate more precise adjustment, the shafts of C9 and C10 are controlled through speed-reducing planetary drives.

(d) Conductance-Zero Circuit

Three stages of adjustment appropriately labeled COARSE, MEDIUM, and FINE are used to obtain both large range and excellent precision. All three stages are resistive dividers between the DRIVE and NULL voltages.

The total range of the CONDUCTANCE-ZERO adjustment is greater than 300 μmho (μsiemens). The shafts of R24 and R25 are controlled through speed-reducing planetary drives; this allows a more precise adjustment of the conductance zero.

2.2 Measurement Accuracy

The use of the BIU places certain constraints upon the range of sample capacitance and conductance values that can be measured and the accuracy with which these measurements can be made. In what follows we shall first consider a simple equivalent circuit for the combination of the sample and the BIU and, second, derive expressions describing the deviation of the apparent or "measured" capacitance and conductance values from the actual values as a function of the equivalent circuit parameters.

(a) Equivalent Circuit

The C/G-meter measures the capacitive and conductive components of a sample admittance Y connected between its terminals, and displays these values on a suitably calibrated linear scale reading directly in units of capacitance (usually pF) or conductance (usually μmho).

Let us define this value of admittance as:

$$\hat{Y} \equiv G + \hat{i}B = G + \hat{i}\omega C, \qquad [1]$$

where B is the susceptance of C.

When the C/G-meter is used with the BIU to measure the same sample, the equivalent circuit is one in which the sample appears to be in series with a resistance R and (possibly) a reactance X. This is illustrated in Fig. 4. The resistance is due principally to the sum of R10 + R11 in Fig. 1. There may also be a small contribution due to the resistance in the windings of L1, L2, L4, and L5, and in the blocking capacitors C3 and C4. The reactance X is equal to the difference between the inductive reactance of the sum of the circuit inductances (L1 + L2 + L4 + L5 + lead inductance) and the capacitive reactance of the series combination of C3 and C4. It was shown in Ref. [1] that there is no advantage to X being capacitive (negative); in practice, we would like it to be either zero

or slightly inductive. We shall, therefore, treat it as if it were due to an "excess" inductance, L.

The admittance $\hat{Y}_A$ "seen" by the C/G-meter; i.e., the *apparent admittance* of the sample, may be written in the form

$$\hat{Y}_A = G_A + \hat{i}B_A = G_A + \hat{i}\omega C_A, \qquad [2a]$$

where

$$G_A = \frac{G(1 + RG) + \omega^2 RC^2}{1 + \omega^2 R^2 C^2 - 2\omega^2 LC + \omega^4 L^2 C^2 + 2RG + (R^2 + \omega^2 L^2)G^2} \qquad [2b]$$

and

$$C_A = \frac{B_A}{\omega} = \frac{C(1 - \omega^2 LC) - LG^2}{1 + 2RG + R^2 G^2 + \omega^2 L^2 G^2 - 2\omega^2 LC + (\omega^2 R^2 + \omega^4 L^2)C^2}. \qquad [2c]$$

Note that Eqs. [2a], [2b], and [2c] consider the effect of sample conductance, G, which in a previous analysis[1] was assumed to be zero.

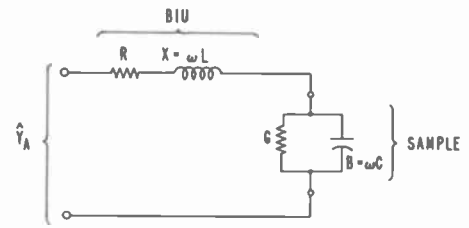

Fig. 4—Simplified equivalent circuit of sample and BIU.

(b) Capacitance Sensitivity Factors

We may define a relative sensitivity factor for capacitance measurements $S(C)$:

$$S(C) \equiv B_A/B \qquad [3a]$$

$$S(C) = \frac{(1 - \omega^2 LC) - LG^2/C}{(1 - \omega^2 LC + RG)^2 + (\omega LG + \omega RC)^2}. \qquad [3b]$$

This gives the ratio of the apparent value of the capacitance C_A that would be measured by the C-meter when used with the BIU to the actual value C that would be indicated by the C-meter alone. In "extended-range" or "modified" MIS $C(V)$ measurements,[2] it is necessary to determine small changes in the capacitance of a sample under test. It is, therefore, of interest to derive an expression for the relative *incremental* sensitivity factor which we shall call $S'(C)$:

$$S'(C) \equiv \frac{dB_A(C)}{dC} \Big/ \frac{dB}{dC} \qquad [4a]$$

$$S'(C) = \frac{(1 - \omega^2 LC + RG)^2 - (\omega LG + \omega RC)^2}{[(1 - \omega^2 LC + RG)^2 + (\omega LG + \omega RC)^2]^2}. \qquad [4b]$$

This gives the ratio of the apparent value of a small change in C that would be indicated by the C-meter when used with the BIU to the actual value of the small change in C that would be indicated by the C-meter alone. Ideally, of course, both $S(C)$ and $S'(C)$ should be equal to 1.00 for all values of C, but this could be true only for L and R equal to zero; i.e., without the protection circuit to which R is essential. The extent to which each of the sensitivity factors differs from 1.00 may be thought of as an *added error* due to the use of the BIU.

It is helpful to consider two separate regimes, $L = 0$ and $L \neq 0$.

(1) $L = 0$

In this regime Eqs. [3b] and [4b] reduce to

$$S(C) = \frac{1}{(1 + RG)^2 + (\omega RC)^2} \qquad [5]$$

$$S'(C) = \frac{(1 + RG)^2 - \omega^2 R^2 C^2}{[(1 + RG)^2 + (\omega RC)^2]^2}. \qquad [6]$$

Clearly, to avoid significant variation of $S(C)$ and $S'(C)$ from 1.00, it is necessary that $RG \ll 1$ and $\omega RC \ll 1$. In previous work involving capacitors fabricated from SOS, the electrode diameter was 0.800 cm, giving an area of 0.5027 cm^2. The anticipated range of sapphire thickness to be used in future measurement was, as discussed in Sec. 1, from 125 to ~400 μm. The maximum capacitance to be expected was, therefore, about 38 pF, using $\epsilon = 10.6\ \epsilon_0$ for the dielectric constant of sapphire. Further, for an MIS sample, it is expected that the maximum value of G *will always be less than* $\omega C/2$.[7] It follows then that for the values $C = 38$ pF and $R = 100$ ohms (see Fig. 1 and Table 1), the upper bounds on the maximum expected values of RG and ωRC would be $(\omega RC)_{MAX} \cong 0.024$ and $(RG)_{MAX} \cong 0.012$.

This could result in a significant error in $S(C)$ and $S'(C)$ if the value of G were to approach $\omega C/2$. Plots of $S(C)$ and $S'(C)$ are shown in Fig. 5 for several values of the parameter $G/\omega C$. Note that for $G/\omega C \lesssim 0.1$, the error in $S(C)$ and $S'(C)$ will be very small.

(2) $L \neq 0$

It is convenient to write eqs [3b] and [4b] in the form

$$S(C) = \frac{1 - \alpha C - \alpha\delta^2 C}{(1 - \alpha C + \gamma)^2 + (\alpha\delta C + \chi C)^2} \qquad [7]$$

$$S'(C) = \frac{(1 - \alpha C + \gamma)^2 - (\alpha\delta C + \chi C)^2}{[(1 - \alpha C + \gamma)^2 + (\alpha\delta C + \chi C)^2]^2}, \qquad [8]$$

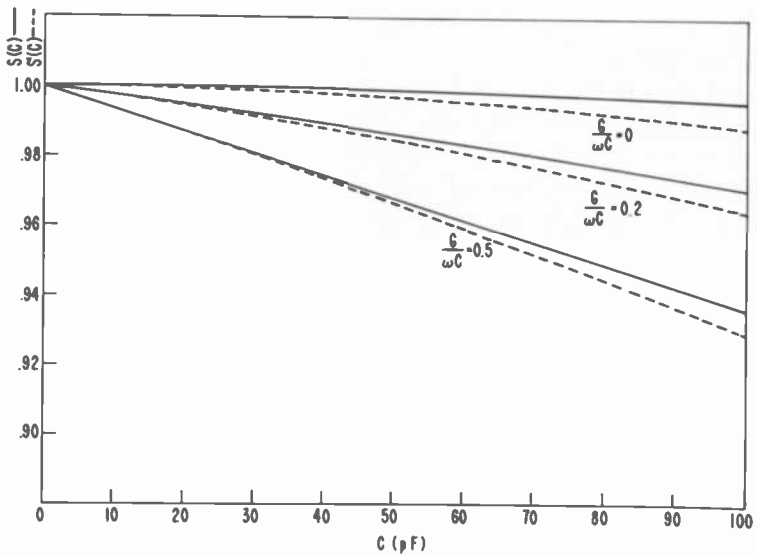

Fig. 5—Relative sensitivity factor $S(C)$ and relative incremental sensitivity factor $S'(C)$ versus C, with R = 100 ohms and $G/\omega C$ as a parameter.

where the definitions and approximate maximum values of αC, χC, γ, and δ in the range $0 < C < 100$ pF are:

$$\alpha C = \omega^2 LC \lesssim 0.02, \qquad [9a]$$

$$\chi C = \omega RC \lesssim 0.06, \qquad [9b]$$

$$\gamma = RG \lesssim 0.015, \text{ and} \qquad [9c]$$

$$\delta = G/\omega C < 1/2. \qquad [9d]$$

Eqs. [7] and [8] may be simplified by carrying out the indicated operations and retaining only linear terms in αC and γ and quadratic terms involving χC:

$$S(C) \cong 1 + \alpha C(1 - \delta^2) - 2\gamma - \chi^2 C^2 \quad [10]$$

$$S'(C) \cong 1 + 2\alpha C - 2\gamma - 3\chi^2 C^2. \quad [11]$$

For nonzero α, both $S(C)$ and $S'(C)$ are increasing functions of C at low values of C, go through maxima, and become decreasing functions at higher values of C. If G were small enough to be ignored, the terms involving δ and γ could be dropped and Eqs. [10] and [11] would reduce to Eqs. [7a] and [7b] of Ref. [1] where the symbol β is used instead of χ^2. It was shown there that an appropriate amount of excess inductance L can be used to increase the measurable range of C without exceeding a set of preassigned error limits on either $S(C)$ or $S'(C)$. The same technique would be applicable here if G were small enough so that δ and γ could either be ignored or limited by smaller maximum values.

(c) Conductance Measurements

Examination of Eq. [2b] reveals that *even when* $G = 0$, there is an apparent conductance G_A due to the series resistance R and the capacitance C. The "contribution" of C to G_A is

$$G_{AC} = \frac{\omega^2 RC^2}{(1 - \omega^2 LC + RG)^2 + (\omega LG + \omega RC)^2}. \quad [12]$$

We may define the "measured conductance" G_M as

$$G_M \equiv G_A - G_{AC}$$

$$G_M = \frac{G(1 + RG)}{(1 - \omega^2 LC + RG)^2 + (\omega LG + \omega RC)^2}.$$

We may use Eqs. [9a] through [9d] to obtain the approximate form

$$G_M \cong G(1 - \gamma + 2\alpha C - 2\chi^2 C^2) \quad [13]$$

and $G_{AC} \cong \omega^2 RC^2(1 - 2\gamma + 2\alpha C - 2\chi^2 C^2)$,

where the expression in parentheses differs from 1.00 by not more than about 4% in the range $0 < C < 100$ pF. Thus, to a reasonable approximation for the present application

$$G \cong G_A - G_{AC} \quad [14]$$

$$\text{and } G_{AC} \cong \omega^2 RC^2. \quad [15]$$

3. Experimental Results

The BIU described in Sec. 2 was tested to ensure that it would properly perform the desired bias-protection (transient-suppression) function and that the accuracy of measurements made with it would not be excessively degraded. These tests and their results will now be described.

3.1 Transient Suppression

The experimental arrangement for testing the transient-suppression capability of the BIU is essentially the same as that shown in figure 6 of Ref. [1]. A test capacitor periodically short-circuiting under high bias (25 kV) is simulated by a motor-driven spark gap. The resulting transient voltage at the C/G-meter BIU output terminals is picked up with a probe and displayed on a fast oscilloscope. The voltage from *each* terminal to ground was checked individually for each polarity of applied bias and was found to have a peak value less than ±110 V without the C/G-meter connected. When the C/G-meter was connected (as shown in Fig. 2b) the peak value of the transient voltage observed at each terminal decreased by more than an order of magnitude. Thus, the C/G-meter is probably overprotected in the sense that R10 and R11 in Fig. 1 are somewhat larger than necessary to achieve the required transient suppression.

In Sec. 2.2 the effect of the BIU on the accuracy of C-meter measurement was considered from a theoretical point of view. The actual effect was determined experimentally by measuring $S(C_S)$ and $S'(C_S)$, where C_S is a standard capacitance for which a precision decade capacitor was used. This 3-terminal capacitance standard has an accuracy of 0.25% for each of its component capacitors. The output of the C-meter was read on the 10-in scale of an X-Y recorder having an accuracy of 0.2% of full scale. Prior to the measurements of $S(C_S)$ and $S'(C_S)$, the C-meter was calibrated on the appropriate scales by connecting the standard capacitor *directly* to the C-meter (i.e., with the BIU out of the circuit), and following the manufacturer's calibration instructions.

After the completion of the C-meter calibration procedure, the standard capacitor was connected to the C-meter through the BIU and through the high-voltage leads connecting the sample holder and test chamber[9] to the BIU. With $C_S = 50$ pF, L4 and L5 were adjusted to make C_A exactly 50 pF. This is equivalent to setting L slightly larger than zero ($L \approx 0.5\ \mu H$).

3.2 Effect of the BIU on the Accuracy of Capacitance Measurements

The value of C_A was then determined as a function of C_S, and $S(C_S)$ was computed for each data point. The results are shown in Fig. 6. Also shown in this figure for comparison are plots of Eq. [5] for $G = 0$ when there is no stray capacitance present and when the stray capacitance C_0 is 50 pF. This will be discussed further in Sec. 5.

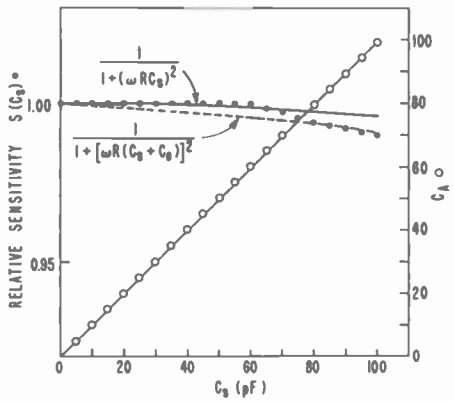

Fig. 6—Plots of C_A versus C_S and $S(C_S)$ versus C_S.

It was not possible to obtain $S'(C_S)$ directly. Therefore, the following approximation was used: $S'(C_S) \cong$ (measured increase in the value of C_A due to an increase of δC_S)/δC_S. For the measurements discussed here, $\delta C_S = 1$ pF. The actual measurement procedure was as follows: (1) a value of C_S was set on the standard capacitor; (2) the capacitance and conductance readings were reduced to zero using the CAPACITANCE ZERO and CONDUCTANCE ZERO controls; (3) the sensitivity of the recorder was increased by a factor such that an additional 1 pF should cause full-scale deflection on the recorder; (4) capacitance and conductance readings were again adjusted to zero; (5) the standard capacitor was increased by 1 pF; and (6) the value of $S'(C_S)$ was read directly from the recorder with full-scale deflection corresponding to $S' = 1.00$. If the deflection exceeded full scale by more than 1% (the available recorder over-range) the sensitivity was reduced by a factor of 1/2, in which case, half-scale deflection corresponded to $S' = 1.00$.

A plot of the experimentally determined $S'(C_S)$ is shown in Fig. 7. For comparison, the figure also shows the theoretical expression, Eq. [6], for $S(C_S)$ based on the simplified equivalent circuit with $L = 0$ and $G = 0$.

The solid line is for the case when the stray capacitance C_0 is zero; the dashed line is for the case when $C_0 = 50$ pF. Clearly neither of these plots is a good fit to the experimentally determined values of S'. This will be discussed further in Sec. 5.

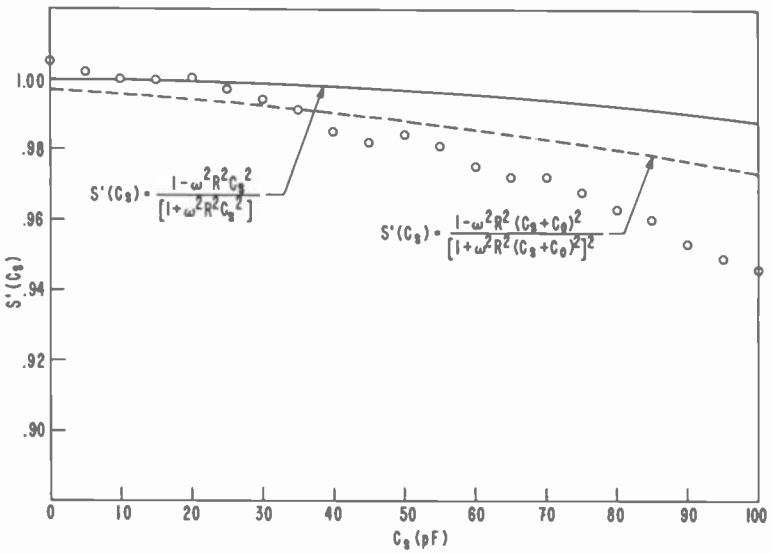

Fig. 7—Relative incremental sensitivity $S'(C_S)$ versus C_S.

3.3 Effect of the BIU on the Accuracy of Conductance Measurements

According to Eq. [15], the apparent conductance due solely to the series resistance R and the capacitance is

$$G_{AC} \cong \omega^2 RC^2.$$

However, C is the sum of the standard capacitance C_S and the stray capacitance C_0. Among the contributions to C_0 are stray capacitances among leads and components in the BIU, capacitance between the sample base in the test chamber and the probe which contacts the sample, capacitance between the high- and low-side leads in the test chamber, and the "zero capacitance" (3 pF) of the standard capacitor when it is connected.

Thus, when the standard capacitor is connected but $C_S = 0$, there is already a contribution to the conductance

$$G_{ACO} = \omega^2 RC_0^2, \qquad [16]$$

which would normally be suppressed by adjusting the CONDUCTANCE ZERO controls to produce a zero conductance reading ($G_A = 0$). Adding increments of C_S should then produce a variation of G_A according to Eq. [17]

$$G_{AC}(C_S) = \omega^2 R(C_0 + C_S)^2 - \omega^2 R C_0^2. \qquad [17]$$

A good fit of Eq. [17] to the experimentally determined variation of G_{AC} (C_S) was obtained for the value $C_0 = 50$ pF. This is shown in Fig. 8. The

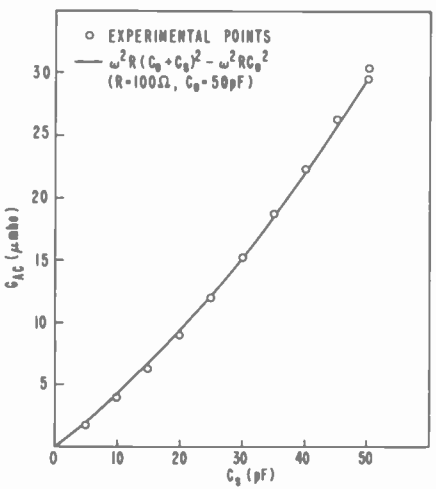

Fig. 8—Apparent conductance G_{AC} versus C_S.

two data points at $C_S = 50$ pF correspond to two different ways of experimentally selecting $C_S = 50$ pF using the precision decade capacitor, viz, 50 pF (lower point) and 30 + 20 pF (upper point).

Selected precision (1% accuracy) film resistors were used as conductance "standards" to check the accuracy of the approximation inherent in Eq. [14]. This was done by using the following procedure: (1) with the standard capacitor connected and $C_S = 0$, C_A and G_A were set to zero; (2) a value of C_S was set on the standard capacitor; (3) G_A was set to zero; (4) a conductance "standard" G_S was connected across C_S and the resultant conductance $G_A - G_{AC}$ was determined. The results were virtually independent of C_S. The largest variation was between the results obtained for $C_S = 0$ and $C_S = 50$ pF; these results are shown in Fig. 9. The results for $C_S = 10$, 20, 30, and 40 pF were intermediate between those for $C_S = 0$ and 50 pF. Thus, the validity of Eq. [14] is confirmed with less than 2% added error in the range $0 < C_S < 50$ pF.

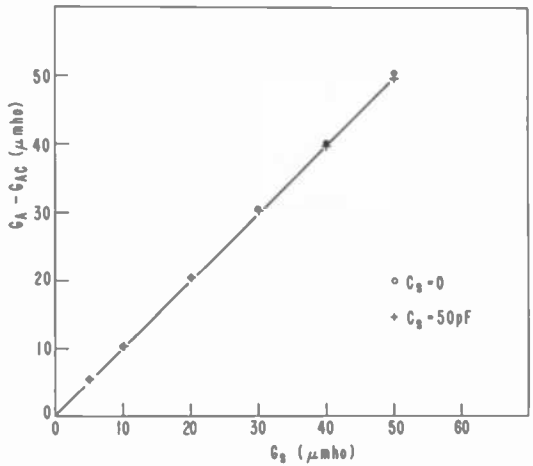

Fig. 9—Conductance $G_A - G_{AC}$ versus standard conductance G_S for $C_S = 0$ and 50 pF.

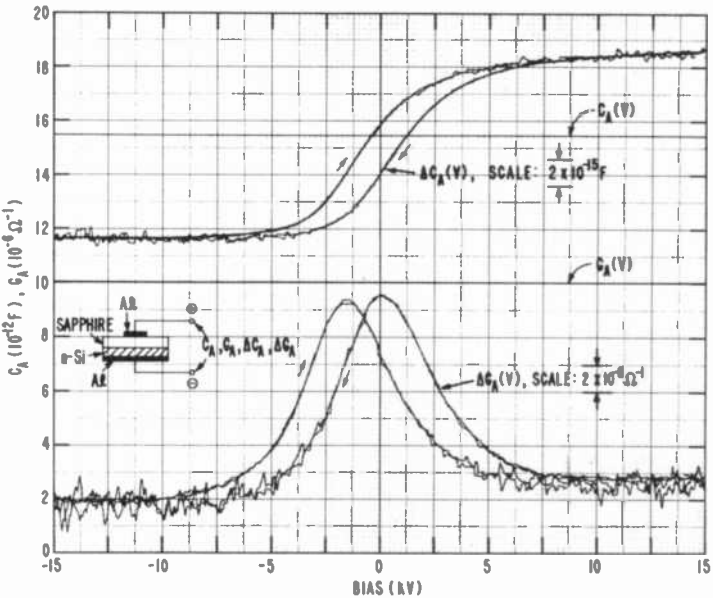

Fig. 10—Variation of capacitance and conductance with bias for an MIS sample fabricated from n-Si on sapphire.

4. Application

An example of a typical application of the C/G-meter BIU is shown in Fig. 10. Here, the results are plotted of MIS $C(V)$ and $G(V)$ measurements versus bias voltage for a capacitor fabricated from n-Si on a sapphire wafer of thickness $\approx 305\ \mu$m. These data are typical of the results obtained thus far with the equipment. The bias range used for this sample, -15 kV to $+15$ kV, is clearly sufficient to cover the desired measurement range. The ± 25 kV capability of the BIU should be more than adequate to cover the bias range required for samples fabricated from Si on sapphire of the maximum thickness currently anticipated ($\sim 400\ \mu$m).

5. Discussion and Conclusions

Although the performance of the BIU is adequate for implementing the desired measurements, there are certain departures from ideality and it is appropriate to discuss them here.

Eqs. [5] and [6] did not exhibit a good fit to the experimentally determined $S(C_S)$ and $S'(C_S)$, respectively, as shown in Figs. 6 and 7. Even when the stray capacitance of ~ 50 pF, as determined in Sec. 3.3 (Fig. 8) was accounted for, the theoretical plots and the experimental data were not in good agreement. Use of Eqs. [3b] and [4b] instead of Eqs. [5] and [6] to take the excess inductance into account would improve the agreement only slightly, at best. However, the simplified equivalent circuit (Fig. 4) used for the theoretical analysis assumes only lumped constant elements. The distributed capacitances and inductances of the actual circuit may contribute significantly to the observed disagreement. Despite this lack of agreement, there is a sufficient range of measurement capability that may be described in terms of an added error due to the use of the BIU. For less than $\pm 1\%$ added error in the measured capacitance C_A, the measurable range of the sample capacitance is found to be from 0 to at least 100 pF. For less than $\pm 1\%$ added error in the measured value of a small change in the sample capacitance, the measurable range of the sample capacitance is found to be from 0 to about 38 pF.

In conclusion: (1) a technique has been described that allows the safe operation of a commercially available C/G-meter for characterization of silicon-on-sapphire by capacitance and conductance measurements at applied-bias voltage levels up to ± 25 kV; (2) the technique requires a bias-isolation unit, whose circuit and theory have been presented together with some practical results.

Acknowledgment

I am indebted to Chester J. Halgas for the mechanical design and the construction of the bias-isolation unit described in this paper, and to James M. Breece for assistance with sample preparation and some of the measurements.

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Aluminum–SOS Schottky Diodes

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Abstract—Aluminum–SOS Schottky diodes having excellent characteristics are described. The series resistance is relatively large, however. The barrier height of the Al–SOS contact is experimentally found to be 0.77 ± 0.02 eV. No degredation in diode characteristics was found when the Al–SOS Schottky diodes were bias-temperature tested at 100°C with V_F = 0.15 V or V_R = 10 V for more than 500 hours.

1. Introduction

During the past ten years Al–nSi Schottky diodes have been studied very extensively. This majority-current-carrier diode has been used in integrated circuits and microwave signal processing. High performance Al–SOS Schottky diodes have potential applications to digital and microwave integrated circuits as well as solar energy conversions. We have fabricated and tested Al–SOS Schottky diodes, and the results obtained are presented here.

The thickness of the SOS films used to fabricate Al–SOS Schottky diodes is 0.6 μm. The concentration of phosphorus in these silicon films is between low 10^{15} to low 10^{16} cm^{-3}. When the doping concentration of the silicon film is too high, the diode has large excess current; when the doping concentration of the film is too low, the diffusion potential of the junction is too small. Thus, a good diode characteristic is difficult to obtain. In addition, the series resistance is large when the doping concentration of the silicon film is small.

The fabrication process is as follows. The silicon islands are defined

and are thermally oxidized. An opening and n+ diffusion are made to provide a good ohmic contact to the n-type silicon film. Oxide at the active diode area is then removed followed by Al metallization. The Al is defined and alloyed at temperatures between 400 to 500°C for 15 to 30 minutes. The process involves only four photomask steps.

2. Current–Voltage Characteristics of Al–SOS Schottky Diodes

The current–voltage characteristics of an ideal Schottky diode is described by Richardson's equation,[1]

$$I = SAT^2 \exp\left(-\frac{q\phi_B}{kT}\right)\left\{\exp\left(\frac{qV_a}{kT}\right) - 1\right\} \qquad [1]$$

where S is the area of the diode, A is the Richardson constant, ϕ_B is the barrier height and V_a is the voltage applied to the metal electrode with respect to the n+ source contact of the diode. The other notations are standard ones. When V_a is positive the diode is forward biased. When V_a is negative the diode is reverse biased. Because of the barrier height lowering effect by the space changes, the actual forward current of a metal–semiconductor diode at intermediate forward bias voltage is given by

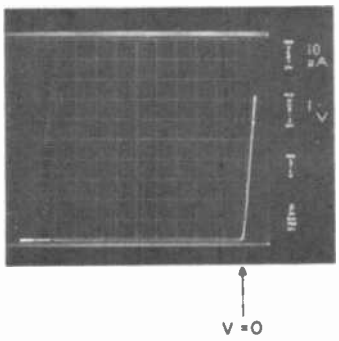
$$I_F = SAT^2 \exp\left[-q\frac{\phi_B - V_F}{nkT}\right], \qquad [2]$$

with n slightly larger than 1.

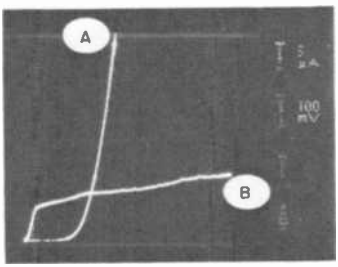
The current–voltage characteristics of a typical Al–SOS Schottky diode is shown in Fig. 1(a). The diode is made on an SOS film 0.6 μm thick doped with 10^{16} cm^{-3} of phosphorus. An excellent rectifier characteristic is shown. The reverse leakage current cannot be seen at the 10 μA/div current scale. The I-V curves are retraced at an expanded scale and are shown in Fig. 1(b). Curve(a) in Fig. 1(b) is the forward current of the diode as a function of forward bias voltage. The scales are shown at the right-hand side of the picture. Curve(b) in Fig. 1(b) is the reverse I-V characteristic of the diode. The current and the voltage scales are 10 nA and 2V per division, respectively. The reverse bias current of the diode at 20 V reverse bias voltage is approximately equal to 30 nA.

The diode current is plotted in a semi-logarithmic paper in Fig. 2. It is obvious that when $V_F \leq 0.2$V the forward current of the diode is approximately given by Eq. [1]. At larger forward bias voltages the series resistance effect becomes important. The series resistance in this particular case is approximately equal to 2,000 ohms. The mask set used in this experiment is a standard MOS field-effect transistor mask set. The

Al contact is made at the drain contact opening where the n+ diffusion is made at the source electrode. If the active diode area is closely surrounded by an n+ diffusion region, the series resistance can be greatly reduced.



(A)



(B)

Fig. 1—The current-voltage characteristics of a typical Al–SOS Schottky diode.

3. Barrier Height

The barrier height of a metal–semiconductor Schottky diode can be obtained from the forward current measurement. This is clearly shown by Eq. [1]. If we extrapolate the linear region of log I_F versus V_F plot to $V_F = 0$, the resulting current I_0 is given by

$$I_0 = SAT^2 \exp(-q\phi_B/kT). \qquad [3]$$

Since only ϕ_B is unknown, the barrier height can be easily calculated. The barrier height of an Al–SOS Schottky diode obtained by this method is equal to 0.78 eV. The barrier height can also be obtained by the mea-

surement of the forward bias current as a function of temperature at a fixed bias voltage, as given by Eq. [2]. We rewrite Eq. [2] as:

$$\log \frac{I_F}{T^2} = \log SA - \frac{q}{nkT}(\phi_B - V_F). \qquad [3a]$$

The activation energy, $\phi_B - V_F$, can be obtained from the slope of $\log I_F/T^2$ versus $1/T$ curve. Fig. 3 presents the experimental result of this

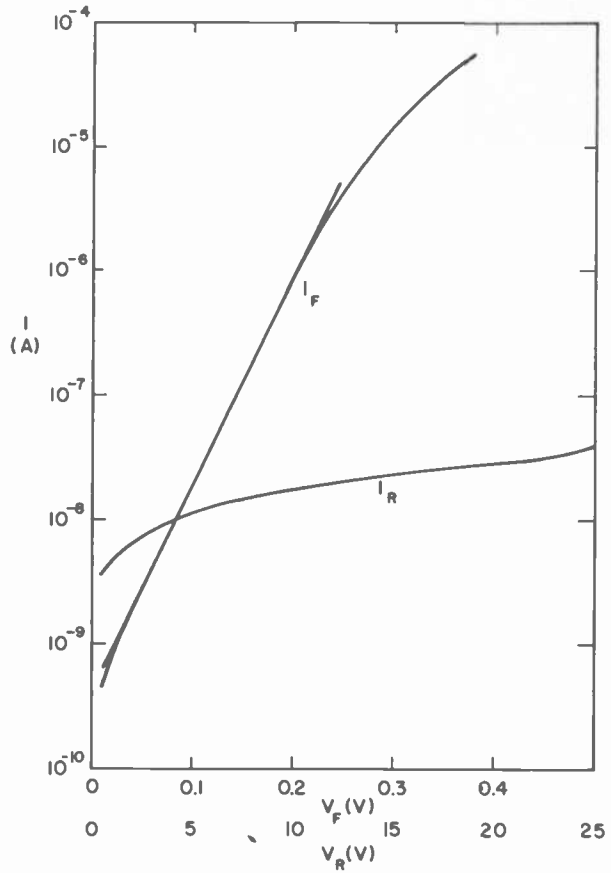


Fig. 2—LogI_F versus V_F plot of a typical Al–SOS Schottky diode.

experiment taken from the diode with $\phi_B = 0.78$ eV as was measured from the I_F versus V_F curve. The forward bias voltage is 0.1 V. The points are measured and the line is drawn to have an activation energy of 0.68 eV, which yields a barrier height of 0.78 eV. It is evident that the

barrier height from these two measurements agree within the measurement error. The barrier height of three batches of Al–SOS Schottky diodes made on silicon films with different doping concentrations has been measured. The barrier height of Al–SOS Schottky diodes is consistently in the range of 0.77 ± 0.02 eV. This barrier height is about 10% larger than that of Al–nSi bulk Schottky diodes as was measured by Yu et al.[2] This can be attributed to the diffusion of Al into silicon film during

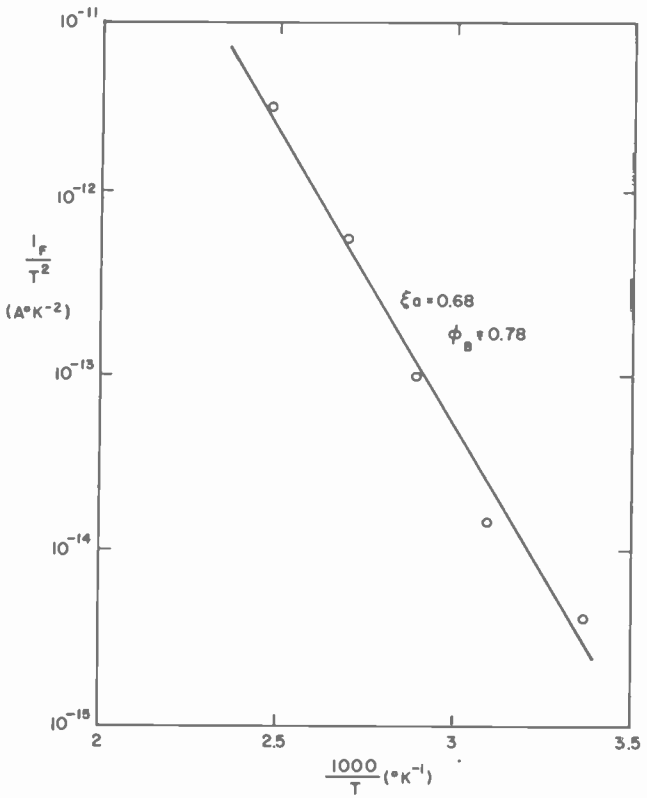


Fig. 3—LogI_F versus 1/T plot of an Al–SOS Schottky diode.

the annealing process. Since Al is a p-type dopant, if a very thin layer of Al is diffused into the silicon films, the contact is actually an Al-p+-n structure. A very thin layer of p+ region increases the actual barrier height of the metal–semiconductor contact.[3,4] The silicon film grown on sapphire substrate has a large lattice strain. This lattice strain enhances the diffusion coefficient of impurities in the film.

4. Bias/Temperature (BT) Tests

We have BT tested Al–SOS Schottky diodes to investigate their stability. The I-V characteristics were measured as the diodes were made and after each successive BT test. The BT test was conducted at 100°C with V_F = 0.15V or V_R = 10V. The results are presented in Figs. 4, 5, and 6. The curves shown in Fig. 4 were taken from a diode as made and after 115, 230, and 660 hours of operation at 100°C with $V_R = -10$V. The line

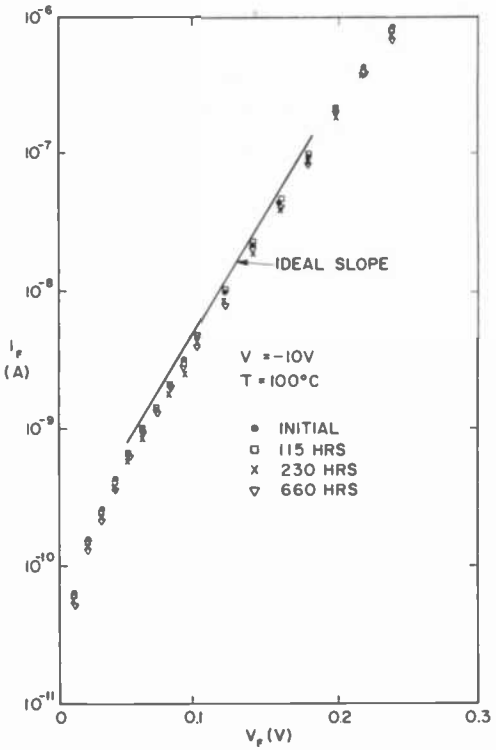


Fig. 4—The forward current-voltage characteristics of an Al–SOS Schottky diode before and after BT tests with $V_R = -10$V.

shows the slope of the I-V characteristics of an ideal Schottky diode with $n = 1$, although the current level is seen to be slightly reduced after BT testing. The decrease in diode current is not significant, since the degradation of the diode characteristic is negligible. Fig. 5 presents the forward diode characteristic for initial operation of a diode with a large amount of excess forward current. The diode is biased with V_F = 0.15V

and operated at a temperature of 100°C. It is clearly shown in Fig. 5 that after the diode has operated for 230 hours at 100°C the excess current is not important. The n factor of the diode forward current is approximately equal to one. A further increase in high-temperature operating time does not change the diode current. Presumable, the diode did not receive adequate annealing during the fabrication processing. The BT test provides an additional heat treatment. After the Al–Silicon contact is properly annealed, the diode current cannot be affected by the high-

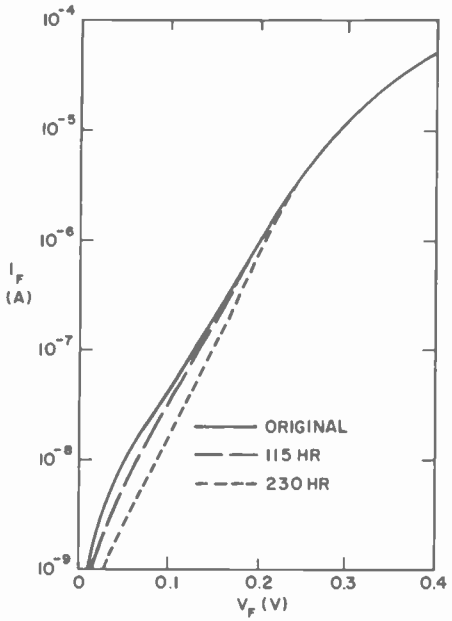


Fig. 5—Forward *I-V* characteristics of a Schottky diode showing the excess current reduced by BT tests.

temperature operation. This is further demonstrated in Fig. 6. The diode whose I-V characteristics are shown in this figure exhibits very small forward excess current. The forward current of the diode after operation at 100°C with $V_F = 0.15$V for 542 hours is the same as that of the diode before it was BT tested. The reverse leakage current of the diode after BT testing is smaller than that before BT testing. In general, it is found that a BT test at 100°C with both forward and reverse biases for 500 hours may change the reverse leakage current of a diode operated at $V_R = 20$V by ±40%. At this time we have no satisfactory explanation of why the leakage current changes in both polarities after BT testing. However,

since the forward current is not effected by BT tests, it is clear that the change in reverse current is due to the effect of Si–SiO_2 or silicon-sapphire interfaces.

Conclusions

We have demonstrated that Schottky diodes can be easily made by depositing Al onto n-type silicon-on-sapphire films. Al-SOS Schottky

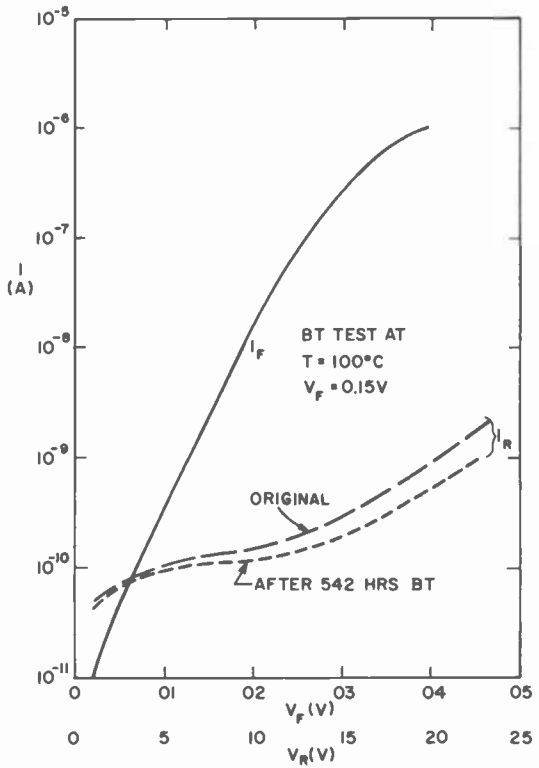


Fig. 6—*I-V* characteristics of a Schottky diode before and after BT tests with V_F = 0.15 V.

diodes follow the forward current of Richardson's equation very well. However, because the thickness of the Si film is only 0.6 μm, the series resistance is large. The series resistance effect can be minimized by proper layout design and by increasing the thickness of the film. The reverse characteristics of the Al–SOS Schottky diodes can be better than that of Al–nSi diodes. This is particularly so when the silicon is very thin.

Since the space-charge at the Al–silicon contact region is small, the barrier lowering by the Schottky effect of the space-charge is small. A larger breakdown voltage can be achieved by simply extending the Al of the Schottky contact to the n+ source region over a thick oxide. At large reverse biases the silicon film between the active diode region and the n+ diffusion region is completely depleted. This depletion region can dissipate a large voltage. Therefore, a large reverse bias voltage can be applied to the diode before the Schottky barrier breakdown. Since the fabrication procedures are very simple, the Al–SOS Schottky diodes can be used to fabricate large scales read only memories.

Acknowledgments:

The author is indebted to M. C. Jones for device fabrications and to J. M. Cartwright for his assistance on the electrical measurements.

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Design Curves for Double-Heterojunction Laser Diodes*

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Abstract—This paper reviews theoretical double-heterojunction laser design curves relating the structure with the transverse mode order able to propagate, the degree of radiation confinement to the active region, the maximum field intensity within the device, and the radiated beam shape. The curves presented are general and applicable to any double-heterojunction structure where the spacing of the heterojunctions and the refractive index in the relevant regions are known.

1. Introduction

This paper reviews design curves relating the heterojunction spacing and index of refraction step with the transverse mode number and radiation pattern of double-heterojunction laser diodes. These curves are based on the treatment of the heterojunction laser as a three-layer dielectric waveguide.[1] Although the first successful heterojunction laser diodes were (AlGa)As/GaAs structures, advances in materials technology have made it possible to construct successful devices using other combinations of semiconductors. The present curves are general and therefore applicable to various material systems.

The key mode-guiding issues of particular interest in laser-diode design are the degree of radiation confinement to the active region, the

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maximum number of transverse modes that can propagate, and the corresponding far-field patterns. In addition, the maximum electric field intensity at the facets is of interest because this may affect the catastrophic-damage limit of the device.[2]

The highest order transverse mode that can propagate in the device depends on the thickness of the waveguide region (determined by the heterojunction spacing) and on the index steps at its boundaries. Information concerning the dominant transverse mode can be deduced from either near- or far-field measurements, but experimental considerations make the far-field the more reliable source. The order of the dominant mode of the cavity can be deduced from the number of lobes in the beam profile. The fundamental mode ($m = 1$) gives rise to a single major lobe, while the mode number for $m > 1$ is given by

$m = 2 +$ (number of low intensity lobes between the two major lobes).

Other useful data deduced from the radiation pattern are the angular separation between the two large lobes and their angular width. The angular separation between the lobes is easily measured and is related here to device parameters.

The index steps at $Al_xGa_{1-x}As/GaAs$ heterojunctions have been experimentally determined from measurements of the refractive index as a function of Al content of (AlGa)As[3] and from heterojunction laser radiation pattern data.[4] Fig. 1 shows the data obtained.

2. Field Description

The electromagnetic mode character discussed here is obtained from a solution of a three layer slab waveguide, Fig. 2. The recombination region 2 (d wide), identical to the optical waveguide, is between two layers having a refractive index smaller than that of region 2. Electromagnetic modes are considered to propagate in the z direction as $\exp[i(\omega t - \beta z)]$, where β is the modal propagation constant. Field variation along y is neglected.

Transverse electric (TE) fields polarized along y predominate in contemporary lasers; consequently, the only nonvanishing quantities are E_y, H_x, and H_z. Equations governing the modes are[1]

$$\frac{d^2E_y}{dx^2} + (k^2 - \beta^2)E_y = 0 \qquad [1]$$

$$H_x = \frac{\beta}{i\omega\mu} E_y \qquad [2]$$

$$H_z = \frac{1}{i\omega\mu} \frac{\partial E_y}{\partial x}, \qquad [3]$$

where $k^2 = \omega^2\mu\epsilon$ is layer dependent, ω is the angular frequency, μ is the permeability, and ϵ is the permitivity.

The solution to Eq. [1] in the various regions is

$$E_{y_1} = A_1 \exp[h_1(d/2 - x)]; x > \frac{d}{2} \qquad [4a]$$

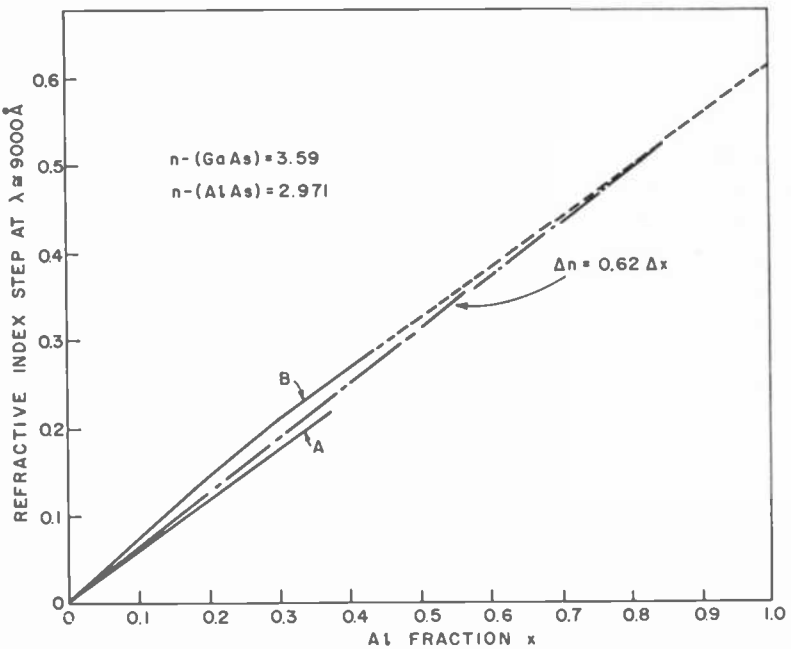


Fig. 1—Refractive index step (at 9000 Å) at an $Al_xGa_{1-x}As/GaAs$ heterojunction as a function of x. Curve A is from Ref. [4] and curve B is from Ref. [3].

$$E_{y_2} = A_2 \cos(h_2 x) + B_2 \sin(h_2 x); |x| < \frac{d}{2} \qquad [4b]$$

$$E_{y_3} = A_3 \exp\left[h_3\left(\frac{d}{2} + x\right)\right]; x < -\frac{d}{2} \qquad [4c]$$

where the transverse wave numbers satisfy in regions 1, 2, and 3

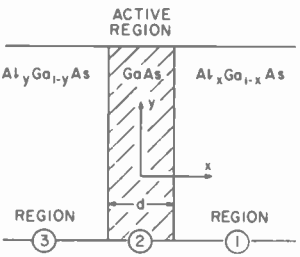
$$\beta^2 - k_1^2 = h_1^2 \qquad [5a]$$

$$k_2^2 - \beta^2 = h_2^2 \qquad [5b]$$

$$\beta^2 - k_3^2 = h_3^2. \qquad [5c]$$

Matching the appropriate field components at $x = \pm d/2$ gives

$$\tan(h_2 d) = \frac{h_2(h_1 + h_3)}{h_2^2 - h_1 h_3}. \qquad [6]$$



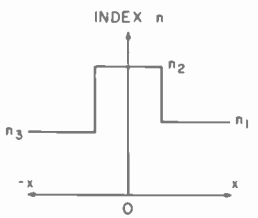


Fig. 2—Three layer dielectric model for the double-heterojunction laser.

The field characteristics of the trapped TE modes can be determined for any set of dielectric steps if the waveguide geometry is normalized. In particular, the quantities h_1, h_2, h_3 and d are normalized,

$$H_i = \frac{h_i}{k_0(\kappa_2 - \kappa_1)^{1/2}}, \; i = 1,2,3 \qquad [7a]$$

$$D = dk_0(\kappa_2 - \kappa_1)^{1/2} \qquad [7b]$$

where $k_0 = 2\pi/\lambda_0$ with λ_0 the lasing wavelength in vacuum and κ_i is the relative dielectric constant of the ith layer.

The secular Eq. [6] then becomes

$$\tan H_2 D = \frac{H_2(H_1 + H_3)}{H_2^2 - H_1 H_3}. \quad [8]$$

The asymmetry factor η is

$$\eta = \frac{\kappa_2 - \kappa_3}{\kappa_2 - \kappa_1} \geq 1. \quad [9]$$

The relations between the normalized parameters are

$$B = H_1 \quad [10a]$$

$$H_2^2 + B^2 = 1 \quad [10b]$$

$$H_3^2 - B^2 = \eta - 1, \quad [10c]$$

where the propagation constant is normalized

$$B^2 = \frac{\beta^2 - k_1^2}{k_0^2(\kappa_2 - \kappa_1)}. \quad [10d]$$

3. Modal Cut-Off Conditions

When the value of H_1 is zero, the field extension along the positive x axis is infinite. This condition defines cut-off for the various trapped modes. To determine the value of D defining cut-off, H_2 and H_3 in Eq. [7] are substituted into Eq. [8] giving

$$\tan D = \sqrt{\eta - 1}. \quad [11]$$

For symmetrical structures, $\eta = 1$ hence $\tan D = 0$. The fundamental mode has no cut-off D value while for mode 2, $D = \pi$. In general, the cut-off D value for the mth transverse mode is

$$D^{(m)} = (m - 1)\pi \quad [12]$$

For a given value of D, the number M of transverse modes is

$$M = \text{In}\left\{1 + \frac{D}{\pi}\right\} \quad [13]$$

where In is the integer truncation of the term in brackets.

For asymmetrical waveguides, the relation [11] is shown in Fig. 3. For a given η value, we find from Fig. 3 the value D' giving the smallest waveguide width at which the fundamental waveguide mode can propagate. The cut-off width for the second mode is $D'' = D' + \pi$; in general, for the mth mode $D^{(m)} = D' + (m - 1)\pi$. The maximum number of propagating modes in a waveguide of normalized width D is

$$M = \text{In}\left\{1 + \frac{D - D'}{\pi}\right\} \qquad [14]$$

As an example, take $d = 5\ \mu\text{m}$, $\lambda_0 = 0.9\ \mu\text{m}$, $n_1 = 3.5$, $n_2 = 3.6$, $n_3 = 3.4$. The asymmetry factor $\eta = 1.96$, and the normalized width $D = 29.4$ and $D' = 0.7782$. The number of possible modes $M = 10$. On the other hand, suppose we wish to design a structure that supports only the fundamental waveguide mode. Then, $D < D' + \pi$, and hence

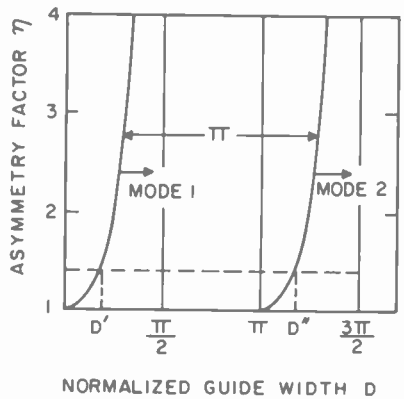


Fig. 3—Cutoff conditions for the first and second waveguide modes as a function of D (see Eq. [7b]). A waveguide geometry defined by a point to the right of each curve implies that the mode can propagate in the guide.

$$d < \frac{\tan^{-1}\sqrt{\eta - 1} + \pi}{2\pi(\kappa_2 - \kappa_1)^{1/2}}\lambda_0. \qquad [15]$$

If we use the index values of the previous example, then $d < 0.67\ \mu\text{m}$.

Fig. 3 shows specific cut-off conditions for the *asymmetric* double-heterojunction laser. We see from Fig. 3 that for $\eta > 4$ the normalized cut-off width D' is relatively insensitive to η variations.

In Fig. 4 we plot three curves defining cut-off for the first four slab-waveguide modes in a *symmetric* DH structure. These curves, obtained from [12], apply to a *lossless* waveguide width normalized to the free-space wavelength. A waveguide defined by a point lying to the right of each curve implies that that particular mode can propagate in the cavity. However, Fig. 4 only provides an approximate guide to the modes actually seen in a laser diode, because our analysis neglects the small contribution of the imaginary part of the refractive index to the dielectric

step associated with a heterojunction. When gain/losses are introduced into the various layers, the dielectric constant has an imaginary part,

$$\kappa_1 \simeq n_1^2 - i\left(\frac{\alpha_1 n_1}{k_0}\right)^2 \qquad [16a]$$

$$\kappa_2 \simeq n_2^2 + i\left(\frac{g n_2}{k_0}\right)^2 \qquad [16b]$$

$$\kappa_3 \simeq n_3^2 - i\left(\frac{\alpha_3 n_3}{k_0}\right)^2 \qquad [16c]$$

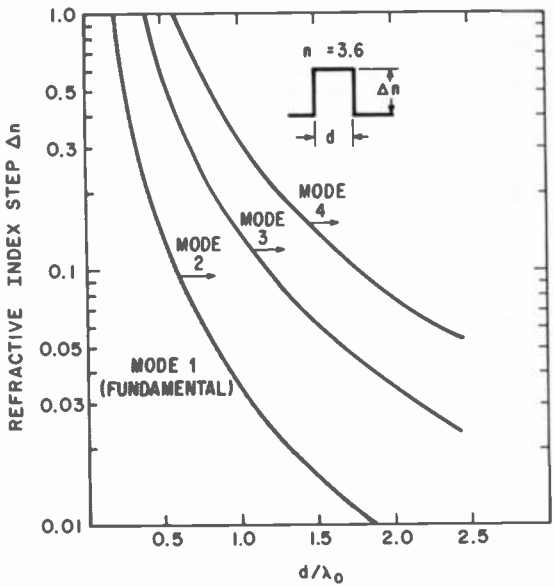


Fig. 4—Modal cutoff conditions for symmetric double-heterojunction lasers. The fundamental mode can propagate for all value of Δn and d/λ_0, but for waveguides defined by points lying to the right of each curve, high order mode propagation is possible.

where α_1,α_3 are the absorption coefficients of the outside regions at the lasing wavelength while g is the gain of the active layer. Consequently, the dielectric step $\kappa_2 - \kappa_1$ will have an imaginary component,

$$\kappa_2 - \kappa_1 = n_2^2 - n_1^2 + i\left[\frac{n_2 g + n_1 \alpha_1}{k_0}\right]. \qquad [17]$$

Since the imaginary parts of κ_1 and κ_2 have different signs, because one

region has loss and the other gain, the imaginary parts are additive in absolute values.

However, the absorption coefficient at the lasing emission wavelength is relatively small in regions 1 and 3 ($<20\ cm^{-1}$) and the gain values in region 2 are moderate (typically under $100\ cm^{-1}$). Therefore, the dielectric difference associated with the third term of Eq. [17] is typically negligible in heterojunction lasers.

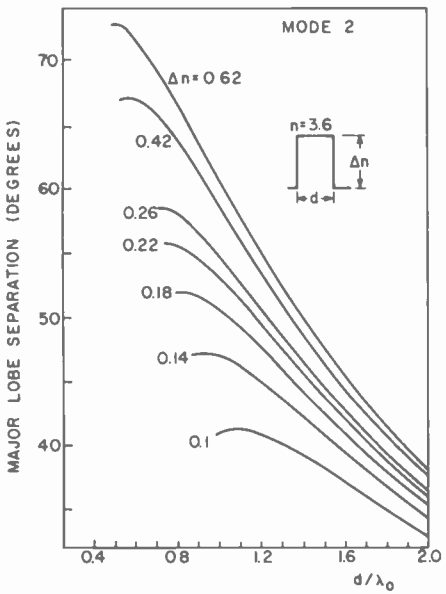


Fig. 5—Major lobe separation in the far-field for device operating in the second mode as a function of the index step Δn and d/λ_0 (symmetric structure).

Finally, the *high-order modes* are characterized by the separations between the two major lobes. In Figs. 5 and 6, we relate the lobe separation to the cavity width with the index step as a parameter. For example, for $\Delta n = 0.18$, $d = 1\ \mu m$ and $\lambda_0 = 0.9\ \mu m$, mode 2 would produce a radiation pattern with a 51° separation between major lobes. However, for the third-order mode, the beam separation between the two major lobes would be approximately 77°.

4. Fundamental Transverse Modes

It is evident from the above that simply increasing the width of the waveguiding region to reduce the beamwidth is not practical. Arbitrarily

increasing the width of two waveguiding region results in the propagation of high-order transverse modes and, consequently, "rabbit-ear" far-field patterns. Conversely, decreasing the heterojunction spacing (while keeping the radiation confinement constant) can decrease the threshold current density, but at the expense of a broad beam.

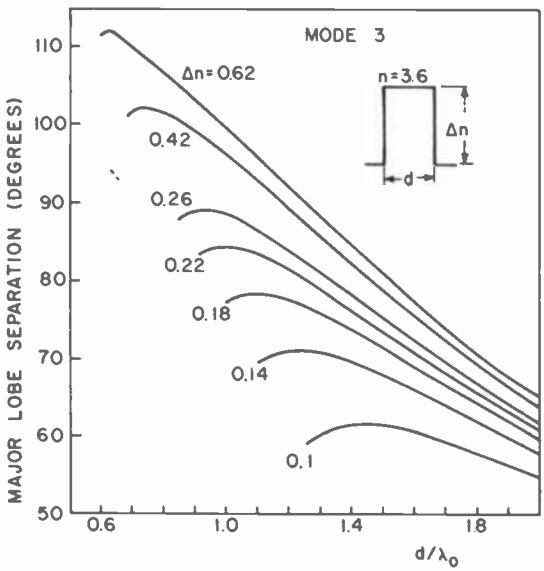
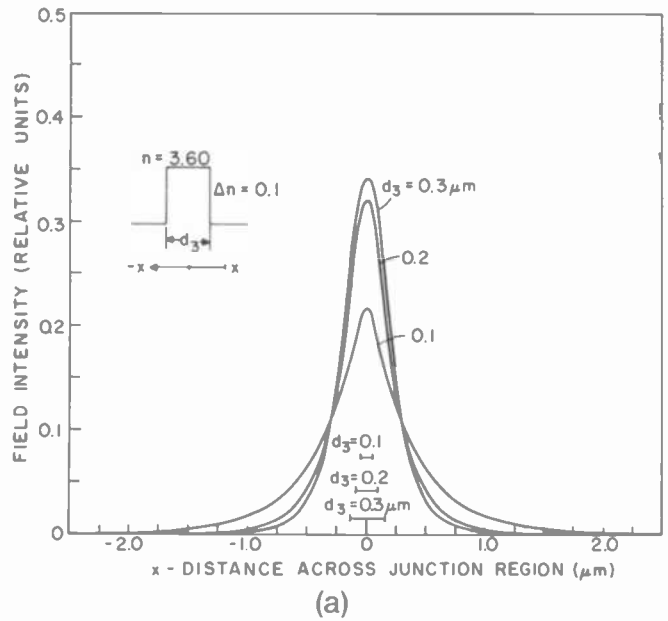


Fig. 6—Major lobe separation in the far-field for device operating in the third mode as a function of the index step Δn and d/λ_0 (symmetric structure).

A practical compromise between low threshold current and moderate beam width is found by using a double-heterojunction laser configuration in which the recombination region (either n-type or p-type) is very narrow and the refractive index steps are moderate, producing optical tails spreading into the adjoining higher bandgap regions.[5,6] This thin DH structure yields a very practical device for efficient room-temperature cw operation.[5]

In the following, we present a series of theoretical plots which show the relationship between the internal device configuration and the near- and far-field distribution. Fig. 7 shows the optical intensity distribution for various heterojunction spacings d with $\Delta n = 0.1$ ($n = 3.6$ in the waveguide region). Since the total optical power carried is the same in each curve, the increase in the peak intensity reflects the increase of field confinement as d is *increased*. Conversely, as d is *decreased*, an in-



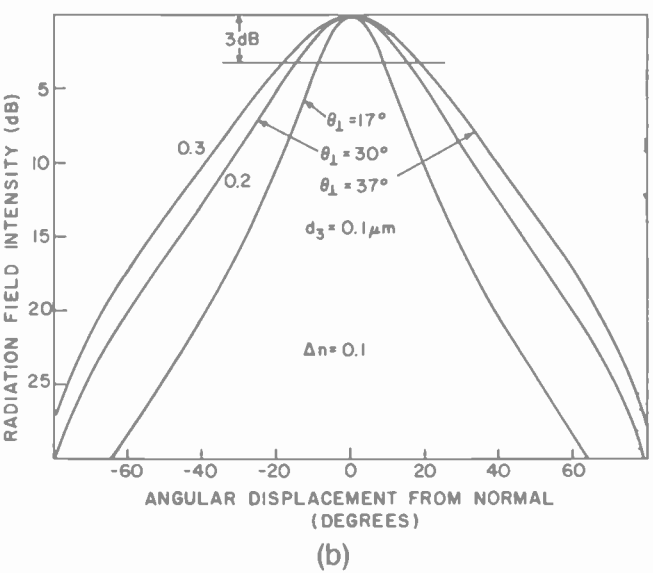
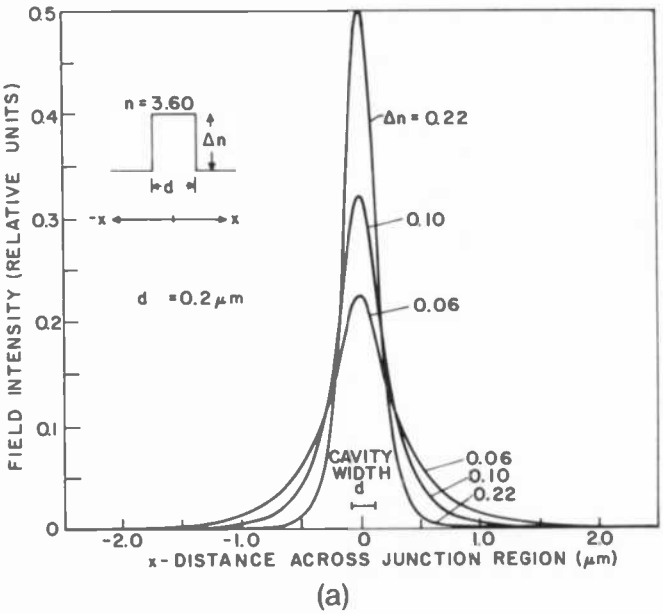
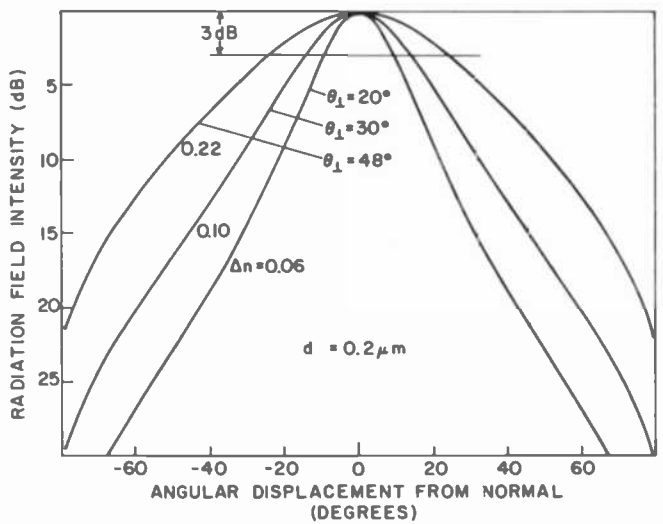


Fig. 7—(a) Field intensity as a function of waveguide width d for $\Delta n = 0.1$; (b) corresponding far-field. Here $\lambda_0 = 0.9$ μm.



(a)



(b)

Fig. 8—(a) Field intensity as a function of Δn for $d = 0.2$ μm; (b) corresponding far-field. Here $\lambda_0 = 0.9$ μm.

creasing fraction of the power propagates outside the region between the heterojunctions. This near-field intensity distribution is reflected in the breadth of the transverse profile of the beam as shown in Fig. 7. The beam width *narrows* as d is decreased because the radiation spreading beyond the heterojunction boundaries increases the source size. In Fig. 8 we show the field intensity plots for various Δn values when $d = 0.2\ \mu m$. The peak field for the structure with $\Delta n = 0.22$ is larger than

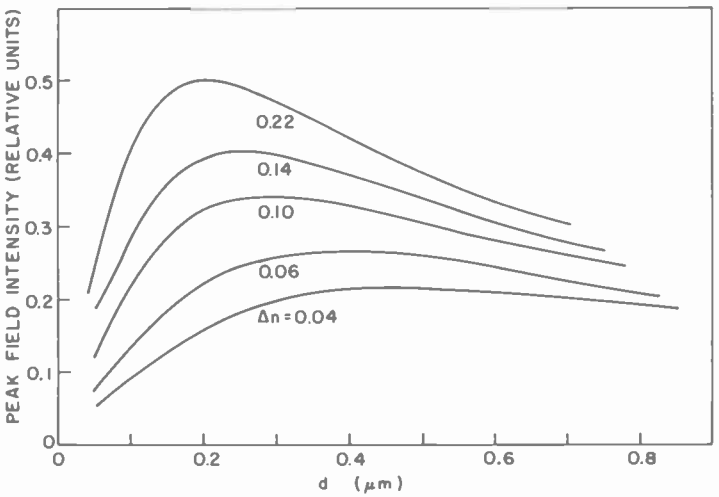


Fig. 9—Peak field intensity as a function of d for several values of Δn. Here $\lambda_0 = 0.9\ \mu m$.

that for the structure with $\Delta n = 0.1$ since the total mode energy for each structure is identical. Fig. 9 summarizes the change in relative peak field intensity within the recombination region as a function of d and Δn.

The dependence of the radiation pattern on Δn and d values of practical interest for DH lasers are shown in Figs. 10 and 11. Fig. 10 shows the dependence of $\theta_\perp$, the half-power beamwidth perpendicular to the junction plane, on the waveguide region width (adjusted for the lasing wavelength) for Δn ranging from 0.06 and 0.62 (which encompasses the complete range in the (AlGa)As alloy system).

The effect of changing the symmetric double-heterojunction laser parameters on the optical confinement factor Γ, representing the fraction of the radiation within the recombination region, is shown in Fig. 11. In Fig. 12 we show the confinement factor as a function of the normalized cavity width D for various asymmetry values.

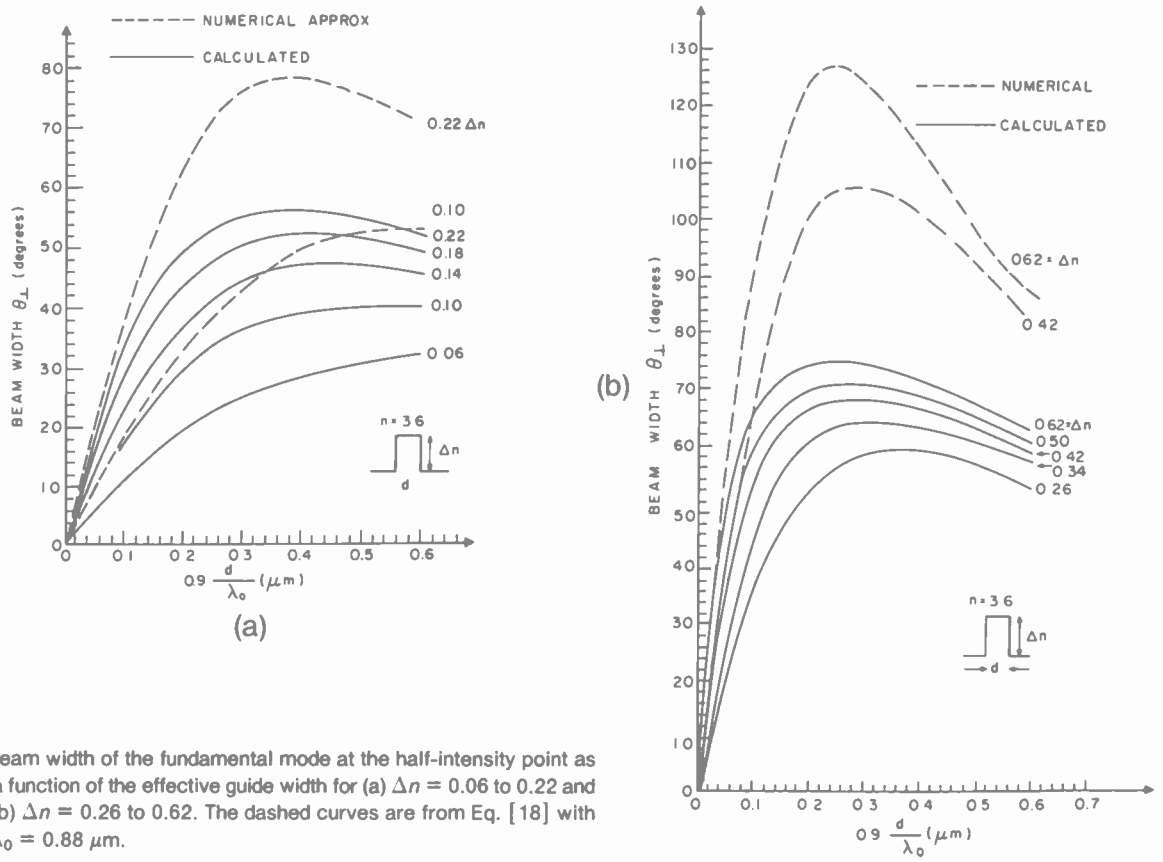
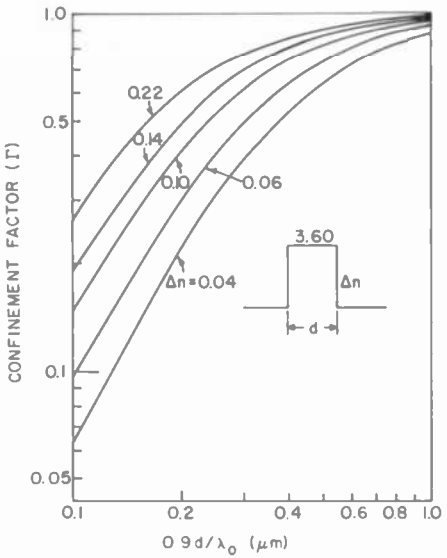
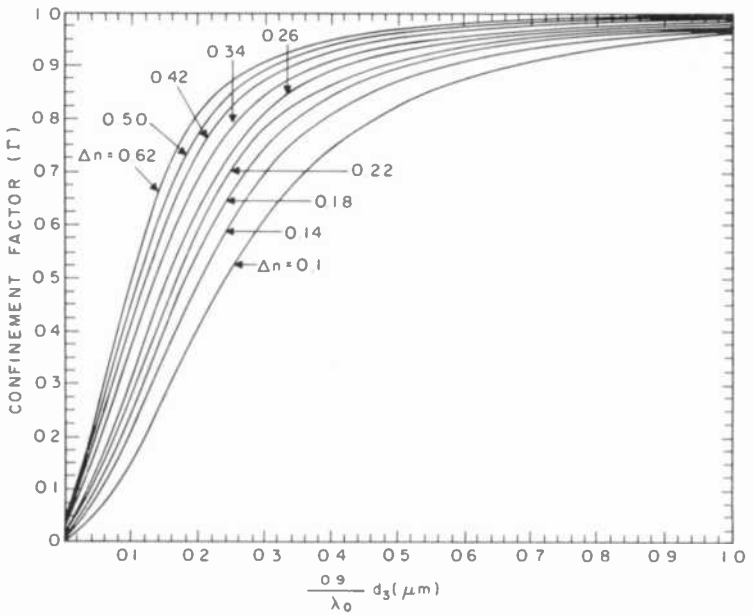


Fig. 10—Beam width of the fundamental mode at the half-intensity point as a function of the effective guide width for (a) $\Delta n = 0.06$ to 0.22 and (b) $\Delta n = 0.26$ to 0.62. The dashed curves are from Eq. [18] with $\lambda_0 = 0.88$ μm.



(a)



(b)

Fig. 11—Wave confinement factor Γ as a function of the effective guide width for (a) $\Delta n = 0.04$ to 0.22 and (b) $\Delta n = 0.10$ to 0.62.

While the curves of Figs. 10 and 11 provide the required information for symmetric device design, it is sometimes useful to have an analytical expression. An expression derived by Dumke[7] for $\theta_\perp$ can be used for small d values ($\lesssim 0.1\ \mu$m),

$$\theta_\perp \cong \frac{Ad/\lambda_0}{1 + \left\{\frac{A}{1.2}\right\}\left\{\frac{d}{\lambda_0}\right\}^2} \text{ (radians)} \qquad [18]$$

where $A = 4.05(n_2^2 - n_1^2)$ with n_2 and n_1 the index values within and outside the recombination region, respectively, at the wavelength λ_0.

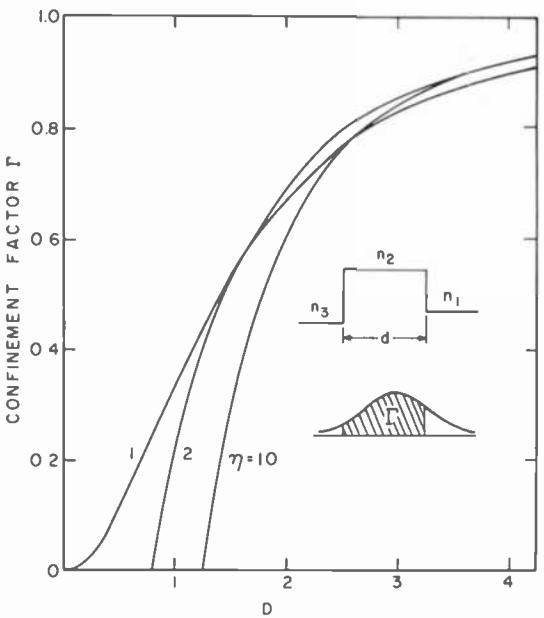


Fig. 12—The wave confinement factor Γ as a function of the normalized guide width D (see Eq. [7b]) for a symmetric DH laser ($\eta = 1$) and asymmetry values $\eta = 2$ and 10.

Eq. [18] is plotted in Fig. 10 where it is compared to the exact computer solutions. It is evident that the $\theta_\perp$ values obtained from Eq. [18] are far too large when d is substantially greater than 0.1 μm, particularly with large Δn values.

An analytical expression also relates the beamwidth to the confinement factor in the range where Eq. [18] is valid,

$$\Gamma \cong \theta_\perp\, d/0.205\, \lambda_0 \qquad [19]$$

where $\theta_\perp$ is in radians. Note that $\Gamma \propto d^2$ for small d.

5. Peak Field at the Facet

The *peak* field strength E_0 in the laser cavity can be estimated from the curves in Fig. 9 in terms of the total radiation power. The fundamental waveguide mode field in a two dimensional slab waveguide is

$$E(x,z) = E_0\psi(x)\exp(-i\beta z) \qquad [20]$$

where the fields are normalized, as in Fig. 9,

$$k_0 \int_{\infty}^{\infty} \psi^2(x)\, dx = 1. \qquad [21]$$

In these symmetric double-heterojunction lasers, the peak field occurs at the center of the active region (at $x = 0$), hence

$$E_{max} = E_0\psi_{max}. \qquad [22]$$

The maximum field at the laser facet can be written in terms of the radiation power per unit length along the facet. The internally incident power P_i at the facet is

$$P_i = \frac{P_\theta}{1 - R}, \qquad [23]$$

where P_θ is the radiated power and R is the facet reflectivity. The field strength E_0 is, therefore,

$$E_0 \sim 10^4 \left|\frac{k_0\eta_0 P_\theta}{(1 - R)n_2}\right|^{1/2} \text{V/cm}, \qquad [24]$$

where P_θ is in watts/μm (power per unit length), k_0 is in μm^{-1}, and $\eta_0 = 120\,\pi$ ohms.

Assume, for example, that the total power uniformly radiated from a 50 μm stripe-contact (AlGa)As laser operating continuously is 5 mW; then $P_\theta = 10^{-4}$ watts/μm. With $\lambda_0 = 0.9\,\mu$m, $E_0 \sim 3.06$ kV/cm. From Fig. 9 we find for $\Delta n = 0.22$ and $d = 0.2\,\mu$m, $\psi^2_{max} = 0.5$. Consequently, the maximum field at the laser facet $E_{max} = (3.06)(0.707) = 2.16$ kV/cm.

Insufficient experimental data exist relating the peak field to catastrophic degradation (which varies with pulse length). However, based on present experience, this peak field value is well within the safe operating limit for cw operation.

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One-Way Doppler Extractor*

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Abstract—This paper presents a feasibility analysis, trade-offs, and implementation for a one-way Doppler extractor system. A Doppler error analysis is discussed that shows that quantization error is a primary source of Doppler measurement error. Several competing extraction techniques are compared and a new "Vernier" technique† is presented that obtains high Doppler resolution with low-speed logic. Parameter trade-offs and sensitivities for this vernier technique are discussed, leading to a hardware design configuration.

Also presented is a performance evaluation of the resulting breadboard model that verifies the theoretical performance predictions. The breadboard model contains the circuitry to interface with an S-band transponder, to extract the Doppler and time interval counts, to compute navigational parameters by means of a microprocessor, and to display the results. Performance tests have verified that the breadboard is capable of extracting Doppler, on an S-band signal, to an accuracy of better than 0.02 hertz for a one-second averaging period. This corresponds to a range rate error of no more than 3 millimeters per second.

1. Introduction

One way Doppler navigation is a technique whereby an orbiting vehicle's position is inferred at the vehicle from a knowledge of the line-of-sight range-rate history to a known reference point. The range-rate history

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† U.S. Patent #3,924,183 assigned to James C. Fletcher, Administrator of the National Aeronautics and Space Administration with respect to an invention by the authors.

is determined by accurately measuring the Doppler shift received from a stable transmitter located at the reference point. Fig. 1 shows the geometrical relationships for a space-vehicle receiver and a ground-based transmitter. The advantage of one-way Doppler navigation is the ability of the space vehicle to determine positional and navigational data autonomously and eliminate the need for special application navigational aids.

One-way Doppler navigation requires very accurate measurements of the vehicle's range rate, with typical values of 3 cm/sec being required over a one-second integration interval. To obtain a range-rate accuracy of 3 cm/sec (0.1 ft/sec) using S-band frequencies, requires that the Doppler frequency be measured to within 0.2 Hz. This in turn requires the use of stable oscillators and accurate receivers as shown in the block diagram of Fig. 2.

The S-band frequency must be controlled to within 0.2 Hz over the period of the Doppler measurement. Also, other error sources such as those caused by Gaussian noise, digital processes, and propagation path variations should be controlled, where practical, to obtain the 0.2-Hz accuracy. The results of the error analysis show that the quantization error resulting from digitizing the Doppler information can be the most significant source of error when conventional frequency-counting techniques are employed. To reduce the quantization error, the Doppler extractor should have some means of determining fractional cycle counts in order that the total error budget be within the required 3 cm/sec (0.1 ft/sec) accuracy.

A new technique has been developed whereby fractional cycle counts

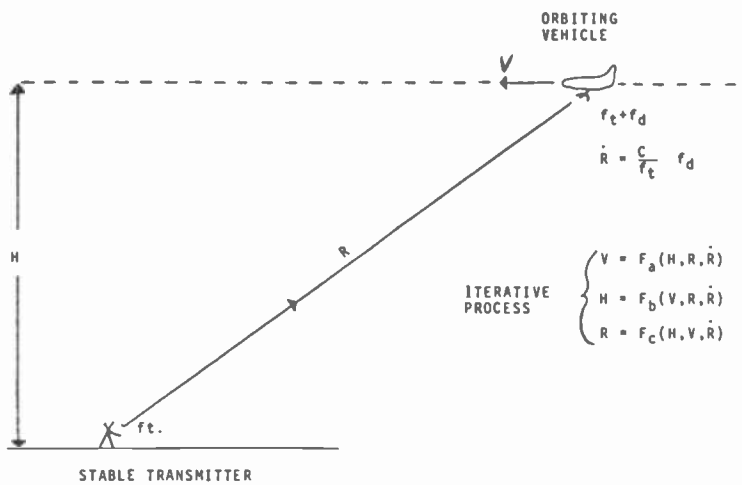


Fig. 1—One-way Doppler geometry.

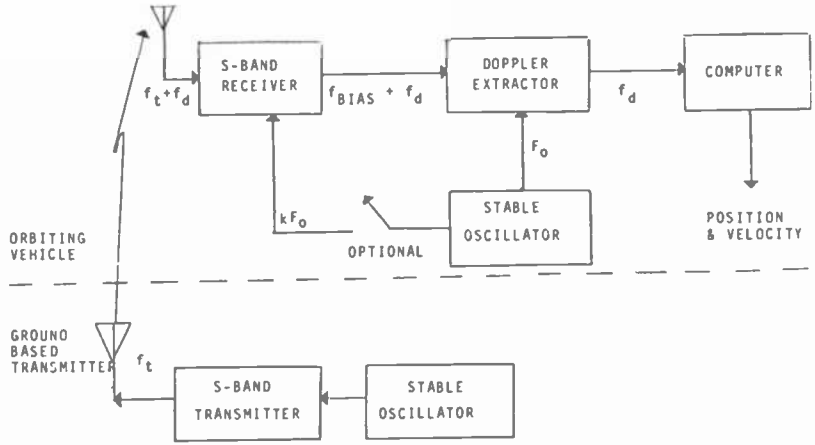


Fig. 2—Block diagram of a one-way Doppler navigation system.

are obtained within short integration periods. This technique employs a vernier approach in that the Doppler frequency is compared with a stable reference oscillator frequency by means of a zero-crossing coincidence detector. The technique offers low weight, low power consumption, and simple construction without sacrificing accuracy or reliability. The analysis and breadboard test results show that it can supply range-rate resolution of at least 3 cm/sec under all reasonable conditions of velocity (0–8230 m/sec), acceleration (0–610 m/sec^2), loop signal-to-noise ratio (>10 dB) and for all integration periods of 0.5 second or more.

The breadboard one-way Doppler extractor is shown in Fig. 3. The functional features of this breadboard are given in Table 1. The breadboard was interfaced with an Apollo USB transponder, operating at a receive frequency of 2101.8 MHz, and with a Univac 1218 computer. The S-band transponder and the associated test instrumentation are also shown in Fig. 3. The breadboard met or exceeded all the work performance requirements shown in Table 2. It was delivered with a 200-nanosecond time aperture setting, which resulted in the performance listed in the last column of the table. As shown, even better accuracy performance can be achieved with a 15-nanosecond time aperture. However, this is at the expense of the delay time between a measurement command and command execution. In applications where the exact time of the measurement's execution is unimportant, this improved accuracy would be readily available.

A preliminary design configuration for flight hardware has been established that satisfies the Rockwell International Space Shuttle requirements. The equipment necessary for Doppler extraction from

Table 1—Breadboard Functional Summary

Parameter	Remarks
Non-destructive readout	Manual or computer selection. Counts continuously for up to 600 seconds with overflow indication.
Destructive readout	Manual or computer selection. Resets counters to zero at start of each new measurement interval.
Fixed integration periods of 0.5, 1, 2, 10, 60 and 600 seconds.	Manual or computer selection of the period with automatic display of results.
Anytime readout	Manual or computer control of the measurement interval from ≈0 to 600 seconds.
Self Test	Injects a known frequency near front end of extractor and checks the computed doppler for accuracy. Test is passed if error ≤0.3 Hz.
Displays	Any one of these results is displayed by push button switches.
Raw bias plus doppler or clock counts.	
Doppler frequency in Hertz.	
Range rate in meters/second.	
Slant range difference in meters	
Time delay between stop command and actual stop execution.	Switch selectable between either display.
Integration time variation in microseconds.	

multiple-carrier-frequency receivers was estimated to be 5.6 × 6.9 × 10.6 inches, weighs 10.2 lbs, and consumes no more than 8 watts of prime power.

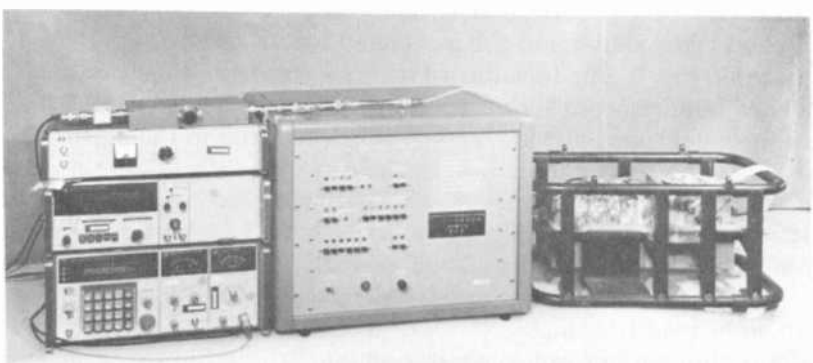


Fig. 3—One-way Doppler extractor breadboard (center) and test instrumentation.

Table 2—Breadboard Performance Summary

Parameter	Work Requirement	Breadboard Performance 15-ns aperture	Breadboard Performance 200-ns aperture
Noise error at the integration period.			
0.5 sec.	0.6 Hz	0.03 Hz	0.24 Hz
2 sec.	0.25 Hz	0.009 Hz	0.05 Hz
10 sec.	0.23 Hz	0.003 Hz	0.01 Hz
60 sec.	0.20 Hz	0.0025 Hz	0.002 Hz
600 sec.	0.20 Hz	0.0025 Hz	0.002 Hz
Maximum time Interval variation	100 μs	60 ms	4 μs

2. Error Analysis

The error budget for a Doppler measuring device consists of three types of errors; deterministic error, bias error, and random error. The sources of these errors and their derivations are described in detail in Refs. [1] and [2]. The deterministic errors are due to predictable effects, such as refraction and multipath. These values can be predicted from estimates of satellite locations, and only residual random errors result. It is assumed that these residual errors are independent between each Doppler measurement, and their contribution to the total error budget is discussed along with the other random error sources.

The bias error does not change significantly during a satellite pass (or longer) and is due to long-term frequency drift of the stable oscillators and uncertainty in the measured value of the speed of light. Since these errors change only slowly with time, if at all, they cannot be removed by filtering (e.g., long averaging times) the individual Doppler measurements. It may be possible to reduce the bias error in predicted range, however, by averaging the predicted location over many satellite passes.

The random errors change between each Doppler measurement (fractions of a second) and are caused by short-term oscillator instabilities, quantization error, phase-lock-loop tracking errors, noise induced errors in the Doppler counter, and residuals from the deterministic errors. These errors can be reduced by some form of filtering (e.g., long averaging times) of each Doppler measurement.

The various errors encountered in the one-way Doppler measurements are summarized in Tables 3, 4, and 5. The quantization error accounts for over 90% of the random error. Thus, techniques that reduce the quantization error would be of significant advantage in controlling the overall error budget for the Doppler extractor.

Table 3—Deterministic Errors

Error Source	Error Magnitude/Remarks
Ionospheric Refraction	Residual error random 1σ = 3.7 cm/sec (0.12 ft./sec)
Tropospheric Scatter	Residual error random 1σ = 6.1 cm/sec (0.2 ft./sec)
Multipath	Requires knowledge of ground station environment.
Vehicle Acceleration	Depends on degree of data processing No error in computed Δ range.

Table 4—Bias Errors

Error Source	Error Magnitude
Measured Velocity of Light	$1\sigma = 3.33 \times 10^{-7}\,\dot{R}$ = 0.28 cm/sec (.009 ft/sec)
Long-Term Oscillator Stability	$1\sigma = C \cdot \hat{S}_{LS}$ = 30 cm/sec (1 ft/sec), $\hat{S}_{LS} \leq 10^{-9}$

Table 5—Random Errors

Error Source	Error Magnitude
Short-Term Oscillator Stability	$1\sigma = C \cdot \hat{S}_S$ = 3 cm/sec (0.1 ft/sec.), ($\hat{S}_S = 10^{-10}$)
Quantization Error	$1\sigma = \frac{C\epsilon}{f_t T\sqrt{6}}$ = 12.2 cm/sec (0.41 ft/sec.), $\epsilon = 1$, $T = 0.5$ sec.
Jitter in Phase Lock	$1\sigma = \frac{C}{2\pi f_t T\sqrt{(S/N)_{loop}}}$ = 1.5 cm/sec (0.05 ft/sec.), $(S/N)_{loop}$ = 10 dB
Noise on VCO Output	$1\sigma = \frac{C}{2.6 f_t T\sqrt{(S/N)\,VCO}}$ = 0.012 cm/sec (0.0004 ft/sec.) : $(S/N)_{VCO}$ = 60 dB

3. Techniques for Reduction of Quantization Error

Several techniques have been investigated for reducing the measurement errors from the Doppler extractor. Of the three primary random error sources, quantization error is the most significant, and many techniques have been devised to reduce this error source as discussed in this section. The other error sources (jitter and frequency stability) can only be reduced by brute-force techniques, i.e., improved S/N ratio, increased averaging time, or improved oscillator stability. These techniques are costly for significant error reduction and require a trade-off of desired accuracy versus cost to achieve that accuracy. The quantization error,

however, can be reduced by proper hardware changes, and the resultant large improvement can be attained with only small changes in cost.

Averaging Time

For reduced quantization error in range rate it is desirable to have long averaging times. However, if the orbiting vehicle is experiencing a changing range rate (acceleration), long averaging times will result in a range-rate error due to the assumption of constant acceleration. This error can be reduced to zero by computing change in range. As the following analysis shows, regardless of the length of the averaging time or the velocity history of the vehicle, the change in slant range is exactly proportional to the change in cycle count:

$$\Delta R_a = \int_0^t \dot{R}\, dt = \text{actual change in slant range.}$$

But

$$\Delta N_d = \int_0^t f_d\, dt = \text{change in cycle count,}$$

and

$$f_d = \frac{\dot{R}}{C} f_t,$$

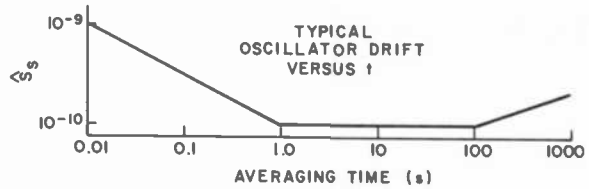
where f_t is the transmitter frequency. Therefore

$$\Delta Nd = \frac{ft}{C} \int_0^t \dot{R}\, dt = \frac{ft}{C}\, \Delta R_a$$

$$\Delta R_a = \frac{C}{f_t} \cdot \Delta Nd \text{ (independent of } t\text{)}.$$

Thus, if changes in slant range are computed, no errors are introduced by using very long averaging times, regardless of the motion of the orbiting vehicle during the averaging period. The change in slant range from the ground transmitter is identically proportional to the change in Doppler count.

Long averaging times will affect the total cycle count if the oscillator drift is significant over the averaging period. For short time intervals, the short-term stability becomes worse as the interval becomes shorter. For many typical oscillators, the stability becomes constant, independent of the averaging time, when the averaging time is in the range of 1 to 100 sec. Fig. 4 shows the results of the most significant errors as a function of averaging time. Above 2.2 seconds averaging time, S_s becomes the dominant error in ΔR, if whole cycles are counted.



Resultant Δ Range Error Versus Averaging Time

t	σR (Drift) (cm)	σR (Quant.) (cm)	σR (Jitter) (cm)	σ RMS (cm)
0.1	0.95	6.1*	0.76***	6.22
0.5	2.10	6.1	0.76	6.50
1.0	3.00	6.1	0.76	6.84
2.0	6.00	6.1	0.76	8.59
5.0	15.00	6.1	0.76	16.21
10.0	30.00	6.1	0.76	30.62
0.1	0.95	0.61**	0.76	1.36
0.5	2.10	0.61	0.76	2.32
1.0	3.00	0.61	0.76	3.15
2.0	6.00	0.61	0.76	6.08
5.0	15.00	0.61	0.76	15.03
10.0	30.00	0.61	0.76	30.02

* Whole Cycle Count ($\epsilon = 1$)
** Fractional Cycle Count ($\epsilon = 0.1$)
*** S/N = 10 dB

Fig. 4—Effect of averaging time on delta range errors.

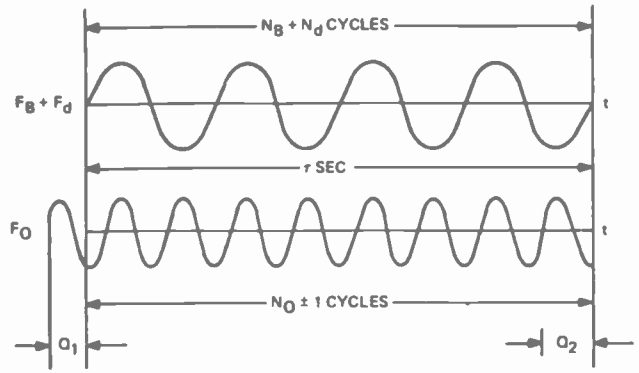
Below 2.2 seconds, quantization becomes the dominant error. If cycles are counted to a resolution of 0.1 cycle, the quantization error is only significant for averaging periods less than 0.1 second.

Period Measurement

W. H. Guier et al describe a technique[3] to reduce quantization error by the method of measuring the period between N cycles of the Doppler frequency (or Doppler + bias). The technique is represented in Fig. 5. The period of N cycles of bias plus Doppler is measured by counting the clock cycles, with a resultant quantization on the clock-cycle count.

The resultant range-rate error is developed in the figure and indicates that the error is reduced by the ratio of the bias to clock frequencies. Thus, for a nominal 1 MHz bias and a 5 MHz clock the range-rate error can be reduced to 2.4 cm/sec (0.08 ft/sec) in a 0.5-second averaging time.

This technique is attractive from the standpoint of simplicity, but the



Error Analysis

$$F_d = \frac{N_B + N_d}{\tau} - F_B = \frac{N_B + N_d}{N_0(1 \pm 1/N_0)} F_0 - F_B$$

$$\epsilon F_d = \pm \frac{N_B + N_d}{N_0^2} F_0 \text{ (Triangular Distribution)}$$

$$\tau = N_0/F_0$$

$$\epsilon F_d = \pm \frac{F_B + F_d}{\tau F_0}$$

$$\sigma F_d = \frac{1}{\tau\sqrt{6}} \cdot \frac{f_B + F_d}{F_0}$$

Fig. 5—Period measuring technique to reduce quantization error.

time interval over which the Doppler count is made becomes a variable. This is due to the fact that N is generally a fixed number and the time required for the Doppler counter to reach N depends on the Doppler frequency. If the bias frequency is 1 MHz and the maximum Doppler frequency is ±60 kHz, then, for a 1-second nominal averaging time ($N_0 = 10^6$ nominal), the actual averaging time would range from 940 to 1060 ms.

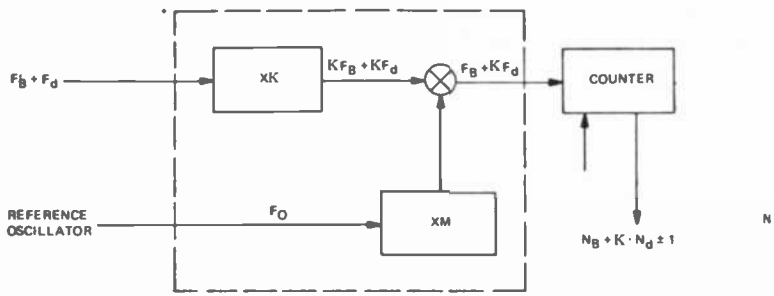
It is possible to reduce the averaging time variation to no more than one period of the bias frequency by making N a variable number. For example, if Doppler frequency is desired at regular intervals (t), the clock counter could output a stop command when the N_ϕ count reaches a pre-determined value (based on t). Both counters would continue to run until the next bias-plus-doppler zero crossing. At this zero crossing both counters would be stopped. The bias-plus-Doppler count would be an exact integer, since its counter would count from exactly one zero crossing to another zero crossing. The clock count, however, would be in error by ±1 count. The time interval variation would be no more than ±1 cycle of the bias frequency.

If the bias frequency were 1 MHz, the time interval would vary no more than ±1 μs. However, a 10-MHz clock and counter would be required to achieve a one sigma Doppler resolution of 0.08 Hz. A lower bias frequency could be used; however, it must be high enough to carry the full range of the Doppler signal. A 100-kHz bias frequency could attain a Doppler resolution of 0.13 Hz minimum (at $F_B + F_D = 160$ kHz) with a 1-MHz clock, but the time interval variation could then be as high as ±25 μs [$1/(F_B - F_D) = 1/40$ kHz].

Frequency Multiplication

Another technique to reduce the quantization error is to multiply the Doppler frequency by some factor (K). For the same time interval, there are K times as many counts, but the quantization error remains at ± one count. In converting to Doppler frequency, range rate, or change in range, the count must be divided by K. Thus, the net quantization error in range rate (for example) is reduced by a factor of K. This technique is represented in Fig. 6.

In the multiplication process the errors due to jitter and long and short-term frequency instabilities are increased by the factor K. How-



Error Analysis

$$Fd = \frac{\frac{N_B + K \cdot Nd \pm 1}{\tau} - F_B}{K}$$

$$\epsilon Fd = \pm \frac{1}{K\tau} \left(\begin{matrix} \text{Triangular} \\ \text{Distribution} \end{matrix} \right)$$

$$\sigma_d = \frac{1}{\tau\sqrt{6}} \cdot \frac{1}{K}$$

Fig. 6—Error reduction by frequency multiplication.

ever, in computing range-rate or change in range the resultant count is divided by K. The errors also are divided by K so that the net result of the multiplication process is that the errors in range rate due to jitter and frequency instabilities are not affected, but the quantization error is reduced by a factor of K. The multiplication process decreases the signal-to-noise ratio by a factor of K^2. Thus, to obtain high resolution (high K), the signal-to-noise ratio (S/N) into the multiplier stage must be high. For example, if $K = 100$, the S/N ratio into the multiplier should be greater than 50 dB if the S/N into the frequency counters is to be at least 10 dB.

The multiplication can be accomplished in alternate stages of multiplication and mixing to prevent the generation of high frequencies. Thus, two decade multipliers and two mixers with 9-MHz reference frequencies could be used to obtain a multiplication of 100 without generating frequencies in excess of 10 MHz (assuming a 1-MHz bias frequency).

Fractional-Cycle Techniques

The fractional-cycle technique employs a high-frequency clock to divide the Doppler cycle into many small fractions. The process is represented in Fig. 7. The fractional-cycle count is used to estimate the Doppler quantization error to within the quantization error of the clock. The resultant improvement is equal to the ratio of the bias frequency to the clock frequency. The errors resulting from jitter and frequency instability are unaffected by this process.

This technique also causes an averaging time interval (t) variation of $\pm$ one bias frequency cycle. To simultaneously achieve high resolution and small time-interval variations, the bias frequency must be large and the clock frequency must be even larger. Thus, a high-speed clock counter must be employed to achieve Doppler resolution improvements of more than about 10. If the bias frequency were chosen to be 1 MHz, the clock frequency would need to be about 14 MHz to achieve a one-sigma Doppler resolution of 0.08 hz. The time-interval variation would be no more than about 1 μs.

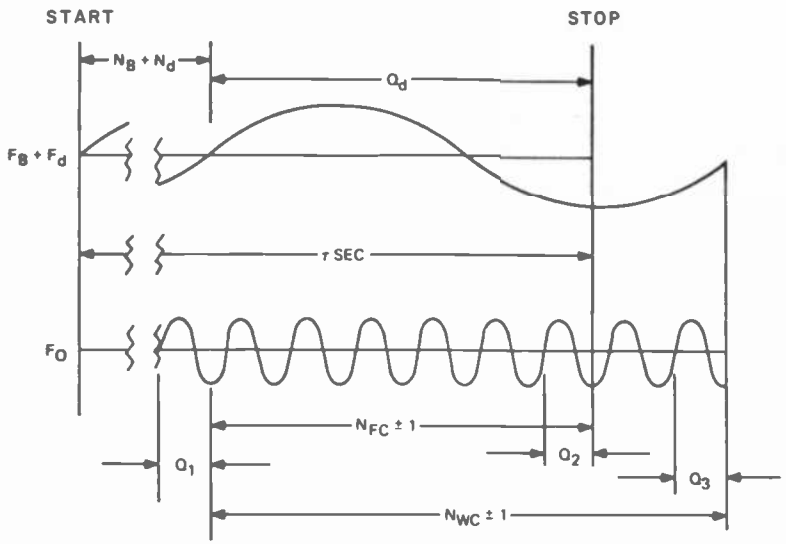
Vernier Technique by Coincidence Detection

The vernier technique is represented in Figs. 8 and 9. This technique employs comparison of zero-crossing coincidences between the bias plus Doppler and clock frequencies to arrive at the Doppler frequency. By counting both frequencies between coincidences, each counter is started and stopped on zero crossings. Thus, the ± 1-cycle count error is eliminated if the coincidence is defined with infinite precision. In practice,

a coincidence would be declared whenever the two zero crossings are within some time interval that is small compared to the period of either frequency. The resultant error in Doppler cycle count is distributed uniformly over the range ± P (where P is the time difference within which the two zero crossings are declared to be coincident). The resultant standard deviation of the Doppler-frequency error is:

$$F_D = \frac{1}{t\sqrt{6}} \frac{2P}{T_{(B+D)}} = \frac{1}{t\sqrt{6}} 2P(F_B + F_D). \quad [1]$$

Since $1/t\sqrt{6}$ is the nominal quantization error, the resultant error is reduced by a factor $2P(F_{(B+D)})$.



ERROR ANALYSIS

Error Analysis

$$Fd = \frac{N_B + N_d + \dfrac{N_{FC} + (Q_2 - Q_1)}{N_{WC} + (Q_3 - Q_1)}}{\tau} - F_B$$

$$\epsilon_{Fd} = \pm \frac{1}{N_{wc}\tau} \left(\begin{matrix}\text{Triangular} \\ \text{Distribution}\end{matrix}\right)$$

$$N_{WC} = Fo \frac{1}{F_B + F_D} = \text{Whole Cycle Count}$$

$$\sigma Fd = \frac{\sqrt{2}}{\tau\sqrt{6}} \cdot \frac{F_B + F_D}{Fo}; \left(\pm \frac{1}{N_{wc}} \text{ at } t = 0, \tau\right)$$

$$\sigma_{r_d} = \frac{1}{\tau\sqrt{6}} \cdot \frac{(F_B + F_D)\sqrt{2}}{Fo}$$

Fig. 7—Fractional cycle techniques to reduce quantization error.

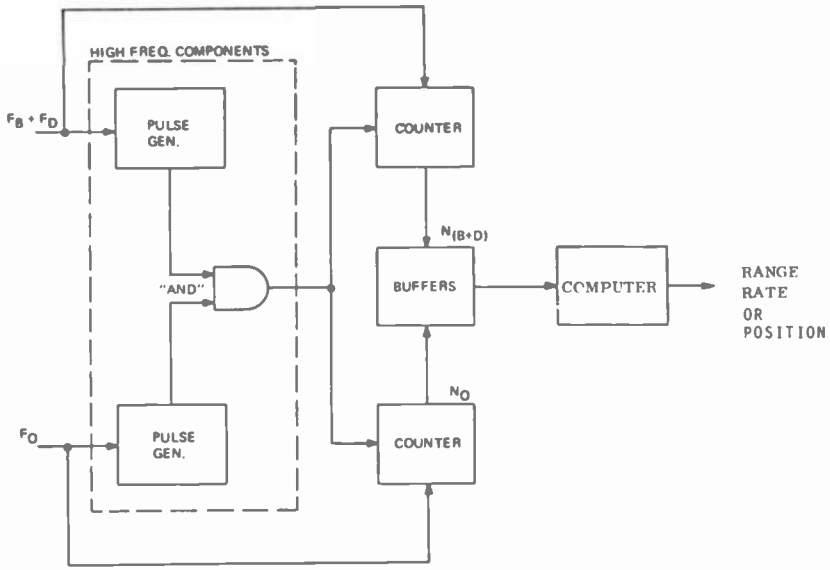


Fig. 8—Coincidence detection Doppler extractor.

The vernier technique has the advantage that high resolutions can be obtained without the need for high-speed counters, since all counted frequencies can be near one megahertz. The time-interval variation occurs with the vernier technique as with some of the other techniques previously described. The time delay depends, in a nonlinear fashion, on the selection of the bias and clock frequencies and the width of the coincidence aperture ($2P$). Typical values of delay are described and shown in a later section.

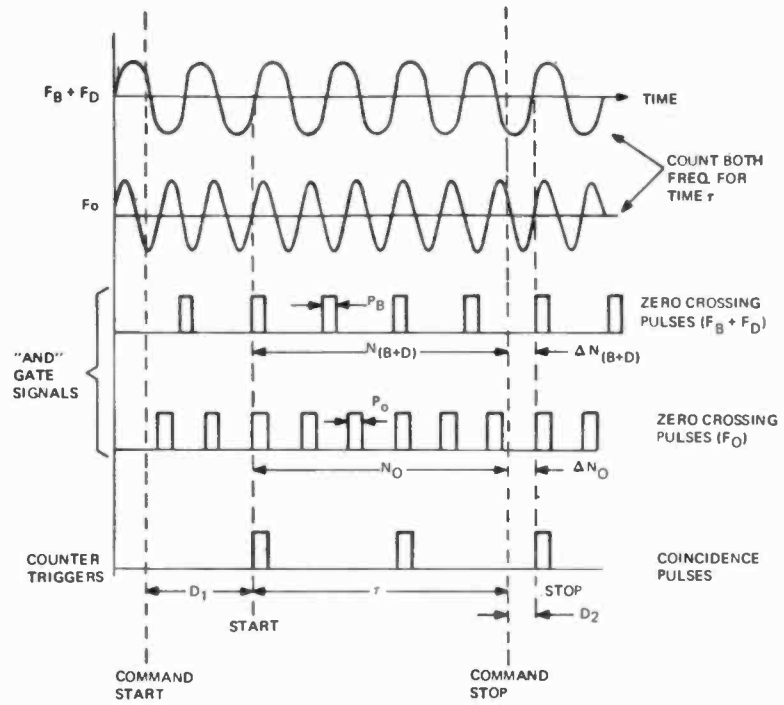
Analogue Technique

The analogue technique employs an energy-storing device to stretch the quantization interval and hence measure it with lower frequency clocks. Hewlett-Packard's computing counter model HP 5360[4] employs this technique using a capacitor as the energy-storing device. Fig. 10 is a functional diagram of the technique. The quantization intervals (T_1 and T_2) are stretched by a factor of 1000 and the clock frequency is counted over the stretched time intervals. The actual period for exactly $N_{(B+D)}$ whole cycles is then

$$\tau = T_0 + T_1 - T_2 = \left(N_0 + \frac{N_1 - N_2 \pm 1}{1000}\right)\frac{1}{F_0} \qquad [2]$$

and

$$F_B + F_D = \frac{N_{(B+D)}}{\tau} = \frac{N_{(B+D)}}{\left(N_0 + \frac{N_1 - n_2 \pm 1}{1000}\right)} F_0. \qquad [3]$$



$$F_D = \left.\begin{array}{l} \tau + D_2 = \dfrac{N_0 + \Delta N_0}{F_0} \\ \dfrac{N_{(B+D)} + \Delta N_{(B+D)}}{N_0 + \Delta N_0} \cdot F_0 - F_B \end{array}\right\} \quad \begin{array}{l} \text{Quantization} \\ \text{Error} = (P_0 + P_B)(F_B + F_D) \end{array}$$

Fig. 9—Timing scheme for coincidence Doppler extractor.

The quantization error is

$$\epsilon_{F_D} = \pm \frac{N_{(B+D)}}{N_0} F_0 \frac{1}{1000\, N_0}. \qquad [4]$$

But

$$N_0 = F_0 \tau$$

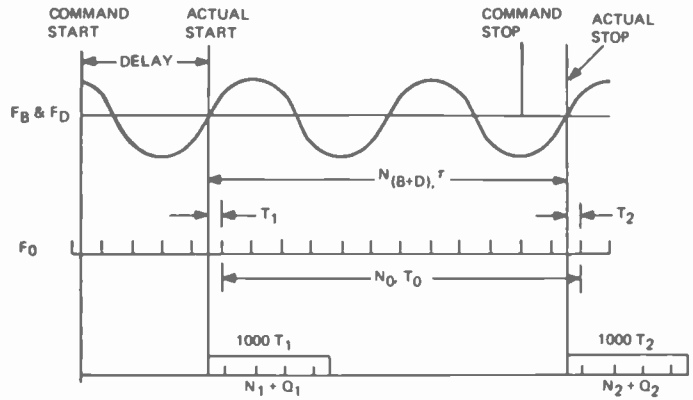
and

$$N_{(B+D)} = (F_B + F_D)\tau; \qquad [5]$$

therefore

$$\epsilon_{F_D} = \frac{1}{\tau} \frac{F_B + F_D}{1000\, F_0} \qquad [6]$$

$$\epsilon_{F_d} = \frac{1}{\tau\sqrt{6}} \cdot \frac{F_B + F_D}{1000\, F_0} \qquad [7]$$



$$\tau = T_0 + T_1 - T_2 = \frac{N_0 + \dfrac{N_1 + Q_1 - N_2 - Q_2}{1000}}{F_0}$$

$$F_B + F_D = \frac{N_{(B+D)}}{\tau} = \frac{N_{(B+D)} \cdot F_0}{\left(N_0 + \dfrac{N_1 - N_2 \pm 1}{1000}\right)}$$

Fig. 10—Analog technique for reduced quantization error.

The quantization error is reduced by a factor of 1000 relative to the nominal counting method. This technique requires that the bias frequency counter begin and end on zero crossings of the bias frequency (since the technique is measuring the period of exactly $N_{(B+D)}$ cycles). The averaging time will vary by one bias frequency cycle, resulting in a delay between the command and the execution of the command similar to other techniques. However, the delay will not exceed one cycle of $F_B + F_D$, or 1 μs, for a nominal 1-MHz bias.

An additional delay in calculating the Doppler shift results from the 1000-times stretching of the clock quantization interval. With the 1000-times expansion, the Doppler shift cannot be calculated until up to 1000 clock periods have elapsed. This could be as long as 1 millisecond if a 1-MHz clock is employed. It is not necessary in the one-way Doppler extractor to use a 1000-fold stretching; a factor of 10 would suffice. Thus, the delay in making a Doppler calculation would then only be 10 μs for a 1-MHz clock.

4. Vernier Doppler Extractor Analysis

The coincidence-detection Doppler extractor was selected to reduce the quantization error without the need for high-speed counters. Even when full Doppler frequencies are available to a conventional counter, the

desired range-rate accuracy of 3 cm/sec (0.1 ft/sec) can only be obtained with integration periods of 5 seconds or longer. Thus, a quantization resolving extractor would be desirable for reduced error at short integration times. The coincidence detection technique is recommended, since this extractor can take advantage of low cost, low power, and high-reliability CMOS components without sacrificing accuracy.

In this section, we analyze the accuracy and time delays associated with the coincidence detection technique and show the limiting effects of this delay on the extractor resolution capability. Also described is the effect of the time delay on the total system errors when the Doppler extractor measurements are compared (or averaged) with other range-rate-measuring equipment (such as accelerometers).

4.1 Extractor Accuracy Analysis

The vernier Doppler extractor uses narrow detection windows to define the coincidence of positive zero crossings of the desired Doppler plus bias frequency and a known reference frequency (stable clock). The principle of operation is similar to that of the familiar vernier caliper measuring instruments, which can obtain a resolving power much greater than the smallest quantized measurement interval. In the vernier Doppler extractor, the positive zero crossings of the signals serve as reference marks, and conventional frequency counters supply the measured cycle counts. If the known and unknown frequency counters are both simultaneously started and stopped on zero crossings, the quantization is eliminated and the unknown frequency can be resolved to a very high accuracy.

Fig. 8 shows a functional block diagram of the implementation required to achieve the coincidence detection and control of the frequency counters, and Fig. 9 shows the resultant signals and timing formats. In Fig. 8, a zero-crossing detector triggers a pulse generator to emit a very narrow and stable pulse at each zero crossing of the unknown and clock frequencies. An "AND" gate detects the coincidence of the pulses when they occur and emits a control pulse to start or stop counters that separately count the unknown and clock frequencies.

Fig. 9 shows how the circuit would operate when discrete measurement intervals are desired. A command to start the counters is received from the computer.

The counters are actually started immediately following the next detected pulse coincidence. Thus, both the bias plus Doppler and clock counters are started immediately after a zero crossing. After a defined measurement period (τ), both counters are commanded to read out the accumulated counts to the computer. The counters, however, continue to count until the next pulse coincidence, at which time the desired

counts are read into buffers. Since both counters were started and read at zero crossings, both counts are very accurate, and the Doppler frequency can be calculated with high precision. The Doppler frequency is given by

$$F_d = \left[\frac{N_{(B+D)}}{N_0} F_0 - F_B\right] \cdot R \qquad [8]$$

where:

$N_{(B+D)}$	=	bias plus Doppler count
N_0	=	clock count
F_0	=	clock frequency and
F_B	=	bias frequency
R	=	Doppler division ratio from the S-Band transponder.

An inaccuracy exists in the counts due to the finite widths of the pulses. Thus, the "AND" gate will respond to a near coincidence if the two pulses overlap to any degree. With reference to the clock count and the pulse rise times, the integer representing the bias plus Doppler count could be in error by a fractional cycle count varying over the range $\pm P/T_{(B+D)}$ cycles, where P is the pulse width from the bias plus Doppler pulse generator, and the clock pulse generator and $T_{(B+D)}$ is the period of the bias plus Doppler frequency.

This error, which occurs at both the start and stop times of the counters, is uniformly distributed over the interval $\pm P(F_B + F_D)$ and each error is independent if τ is much larger than the interval between coincidences. The combined error results in a maximum Doppler error defined by

$$\epsilon F_d = \pm \frac{2P(F_B + F_D)}{\tau} R, \qquad [9]$$

and a standard deviation defined by

$$\sigma F_d = \frac{2P(F_B + F_D)}{\tau\sqrt{6}} R, \qquad [10]$$

where R is the ratio of S-band Doppler to counted Doppler and τ is the measured period.

If the Doppler extractor were only concerned with obtaining an accurate Doppler measurement over a period of 1 second, say, with no regard to how much the 1-second time interval could vary, then P could be made arbitrarily small. A one-ns pulse, for example, and a 1-MHz bias frequency would result in a Doppler error of 0.002 cycle or 0.002 Hz in a second period, provided full doppler is available into the Doppler counters ($R = 1$). Such a pulse width is feasible with stable rise times of 0.1 ns.

4.2 Time-Delay Analyses

A coincidence of zero crossings occurs whenever the two pulses have some overlap into the "AND" gate. The probability of a coincidence depends on the pulse widths and the interpulse periods. The average period between coincidences can be shown to be given by

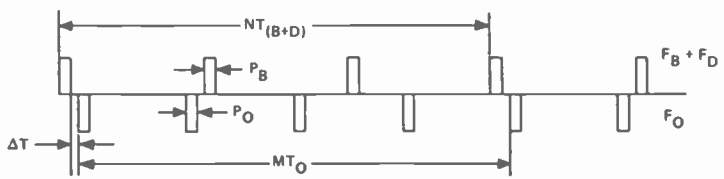
$$\overline{T}_c = \frac{1}{(P_0 + P_B)(F_B + F_D)F_0}. \qquad [11]$$

This formula assumes that the clock and bias-plus-Doppler frequencies are not harmonically related or, if so, enough random variation in their frequencies is present to assure that the maximum period between coincidences is not excessive.

If the bias plus Doppler frequency is an exact rational fraction of the clock frequency, a coincidence may never occur if the pulse width is made too narrow. This is shown in the diagram of Figure 11.

If the frequency ratio $(F_B + F_D)/F_0$ is defined by the integers N/M (N/M is reduced to its lowest form and $N < M$), a coincidence will occur in MT_0 seconds if the pulse width is greater than or equal to $T_0/2N$ (T_0 = clock period). With $P = T_0/2N$, the Doppler error equation becomes

$$\epsilon F_D = \pm \frac{2P(F_B + F_D)}{\tau}, \qquad [12]$$



$M \approx N$; $M > N$; M & N Exact Integers

When

$$\frac{F_B + F_D}{F_0} = \frac{N}{M},$$

then

$$T_{(B+D)} = \frac{M}{N} T_0 \ (M \text{ \& } N \text{ have no common factors}).$$

Maximum possible separation at point of closest coincidence is given by

$$\Delta T \leq \frac{1}{2N} T_0 - \frac{(P_0 + P_B)}{2}.$$

Coincidence will occur in $M\,T_0$ seconds if

$$\frac{P_0 + P_B}{2} \geq \frac{T_0}{2N}.$$

Fig. 11—Effect of resonances in coincident detector.

but $2P = T_0/N$ and $F_B + F_D = (N/M)F_0$ (by definition). Therefore

$$\epsilon F_D = \pm \left(\frac{T_0}{N}\right)\left(\frac{N}{M}F_0\right) = \pm \frac{1}{M\tau}; \text{ since } T_0F_0 = 1. \qquad [13]$$

M is the resolving power of the vernier extractor. The time delay has a maximum value of

$$t_{d\text{MAX}} = MT_0 \ (t_d \text{ is uniformly distributed from zero to } MT_0).$$

Since the time delay is random, the actual measurement interval can vary from $t - MT_0$ to $t + MT_0$. To keep the time interval variation small M should be small. But for high doppler accuracy M should be large. Thus, a compromise is required between acceptable time interval variations and desired Doppler measurement accuracies.

Thus, for any given bias and clock frequencies, a minimum pulse width exists ($P \geq T_0/2N$) which will guarantee a coincidence in a short time interval (from 10 to several hundred clock periods). For highest resolution and shortest time delay, the bias frequency should be chosen as close to the clock frequency as the doppler variation will allow. This is analogous to the mechanical vernier caliper, which has one scale only 10% larger than the other scale. When the bias frequency is chosen to be 100 kHz below the clock frequency (the bias frequency carries ±60 kHz of Doppler variation), the minimum allowable pulse width decreases as the clock and bias frequencies are increased. To achieve the highest resolution and shortest time delays the clock and bias frequencies should be chosen as large as possible and the pulse widths as narrow as possible. Fig. 12 shows the sensitivity of the Doppler resolution to the clock reference frequency when the bias frequency is chosen to be offset from the clock frequency by 100 kHz. As shown in the figure, Doppler resolution to 0.02 cycle can be obtained with a maximum possible delay of 25 μs, if the clock and bias frequencies are chosen at about 10 MHz. The pulse width, under these conditions would need to be one nanosecond.

5. Breadboard Design

The Doppler extractor breadboard implemented uses the vernier extractor technique to resolve the quantization error. The breadboard unit accepts a 76.083-MHz signal from an S-band transponder and contains the necessary circuitry to perform rf and digital processing to extract the Doppler and Doppler-related information from the input.

The rf processor translates and multiplies the input frequency to obtain a suitable bias frequency containing approximately the full S-band signal. It also generates a self-test signal for the self-test modes. The digital processor performs the functions of coincidence detection,

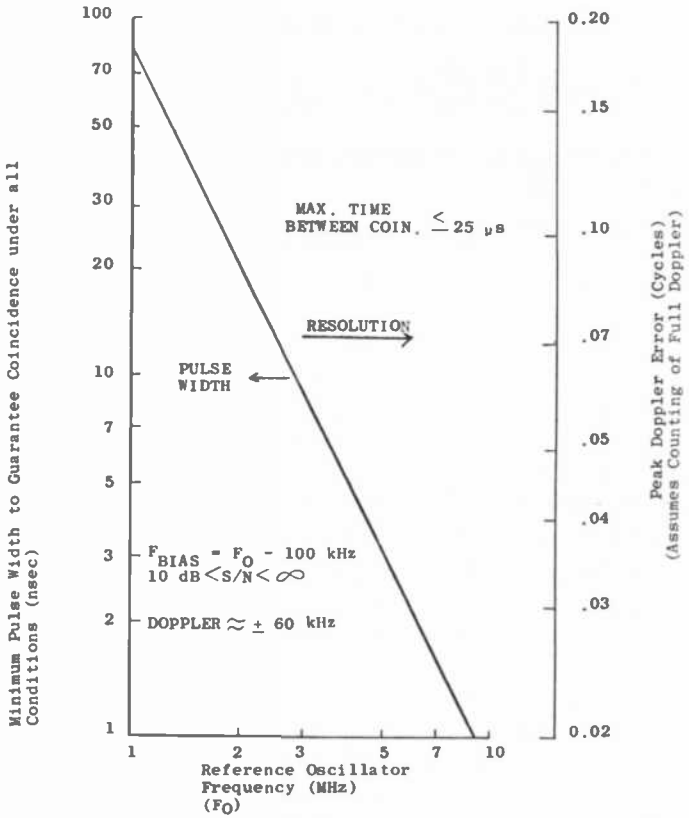


Fig. 12—Minimum pulse width to guarantee coincidence for all conditions.

digital counting, timing, data processing and display, and interface formatting for a UNIVAC 1218 computer. The unit also contains a microprocessor for calculations of the displayed data and for self-test analysis. A view of the extractor chassis is shown in Fig. 13. The rf and digital processing subchassis are indicated.

5.1 Technique Description

A diagram of the one-way Doppler extractor interfaces is shown in Fig. 14. The S-band transponder receives the Doppler-shifted transmitted frequency and outputs a 76.083 MHz reference signal containing 8/221 parts of the original S-band Doppler. The Doppler extractor performs rf processing to restore approximately full Doppler on a 1-MHz bias frequency and performs digital processing to extract Doppler counts, time interval counts, display data, and computer interface logic to a

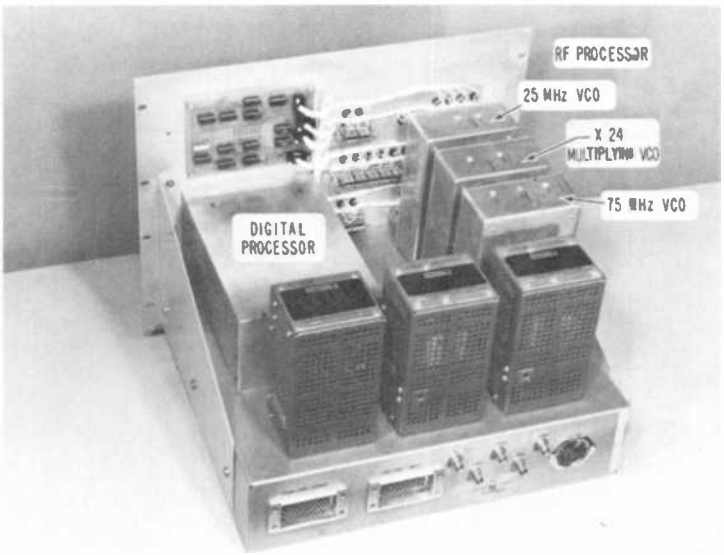


Fig. 13—One-way Doppler extractor chassis.

UNIVAC 1218 computer. The timing circuits operate from an external 5-MHz frequency standard.

Fig. 15 is a block diagram of the extractor, showing some of the internal functions performed by the rf and digital processors. As shown, the transponder signal enters the rf processor, which performs frequency shifting and multiplication resulting in a Doppler shift up to ±60 kHz

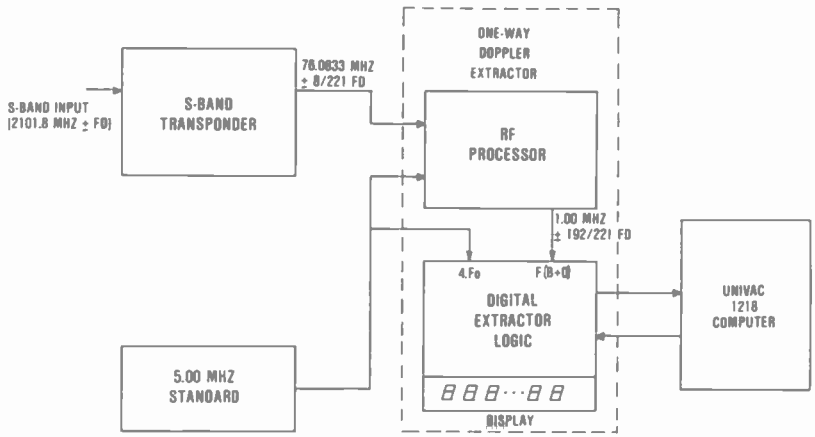


Fig. 14—One-way Doppler extractor interfaces.

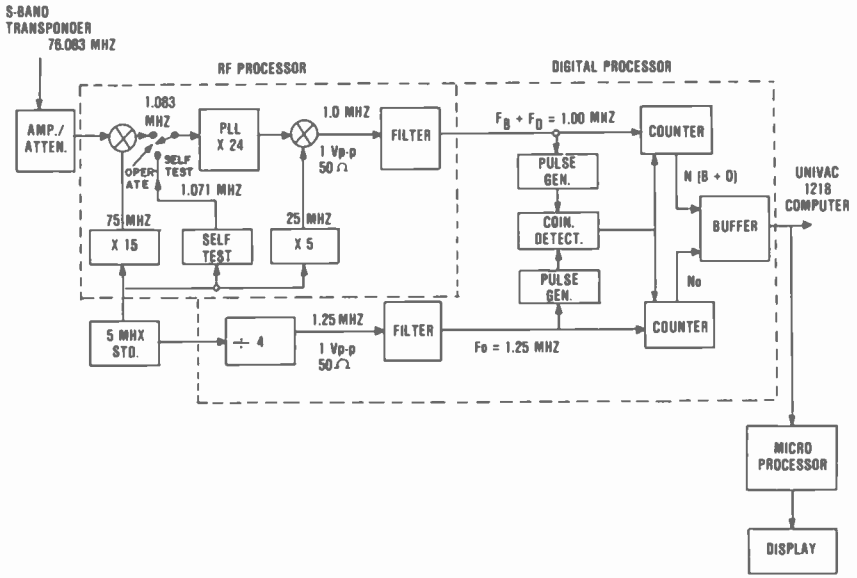


Fig. 15—One-way Doppler extractor breadboard block diagram.

superimposed on a 1.00-MHz bias signal. The 76.083 MHz is mixed with a 75-MHz fixed injection frequency to obtain a 1.083-MHz plus fractional Doppler ($f_d/27.625$) S-band reference signal. This frequency is then multiplied by 24, resulting in a 26-MHz output containing 192/221 parts of the original S-band Doppler shift. The 26-MHz signal is then mixed with a 25-MHz fixed injection to obtain the desired 1 MHz containing nearly the full S-band Doppler shift. The coincidence clock frequency (F_0) of 1.25 MHz is obtained by dividing the 5-MHz clock by a factor of 4.

The above frequencies were chosen for the breadboard unit for the following reasons:

1. The coincidence clock and bias frequencies should be approximately equal and at about 1 MHz for best utilization of CMOS logic and the coincidence technique.

2. The injection frequencies should be low integer multiples of the clock for ease of generation and to obtain very clean injection frequencies.

3. The multiplying phase locked loop should have a multiplication factor that restores most of the original S-band Doppler.

Other frequencies could be used in the extractor at the expense of increased circuit complexity.

The digital processor circuits of Fig. 15 contain the pulse generators and coincidence detector required for the vernier extractor concept. The

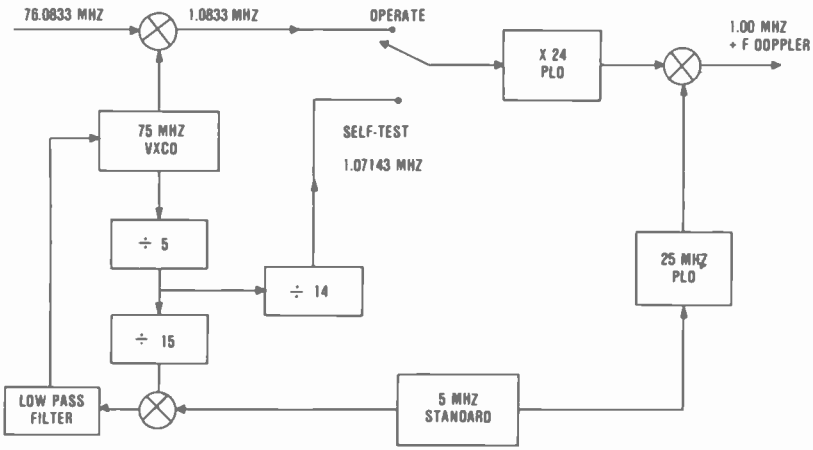


Fig. 16—Self-test implementation block diagram.

bias-plus-Doppler and coincidence clock frequencies are converted to narrow pulses at each zero crossing, and these pulses are fed to the coincidence detector. The coincidence detector responds to a pulse coincidence by generating a timing pulse. This pulse plus internal timing logic causes the counters to transfer their counts to the buffers at desired intervals. At coincidence, the quantization error is reduced to a small timing error due to a finite pulse width.

Two counters count zero crossings of the F_{B+D} and F_0 signals. For nondestructive readout (NDRO), the counters run continuously. For destructive readout (DRO), the counters are reset at the beginning of each count interval. The two counter outputs ($N_{(B+D)}$ and N_0) are stored in the buffers for computer sampling as desired. The buffer circuits also contain interface circuitry to convert the counts into coded words for the UNIVAC 1218 computer.

The self-test function tests the operation of the Doppler extractor from the output of the first mixer to the computer interface. A block diagram of the technique is shown in Fig. 16. A test frequency is obtained from the 75-MHz first mixer injection oscillator by dividing this frequency by 70. Derivation of the test frequency from the 75-MHz oscillator is preferred over up converting from the 5-MHz standard, since the former technique also tests the lock condition of the 75-MHz oscillator to the 5-MHz standard. The resultant frequency of 1,071,428.57 Hz is substituted for the nominal mixer output frequency of 1,083,333.33 Hz. After multiplication by 24 and differencing with the 25-MHz injection frequency, the resultant bias-plus-Doppler frequency into the coincidence detector is 714,285.7 Hz. Since the nominal bias frequency is 1 MHz, the resultant equivalent Doppler frequency at the extractor display will be

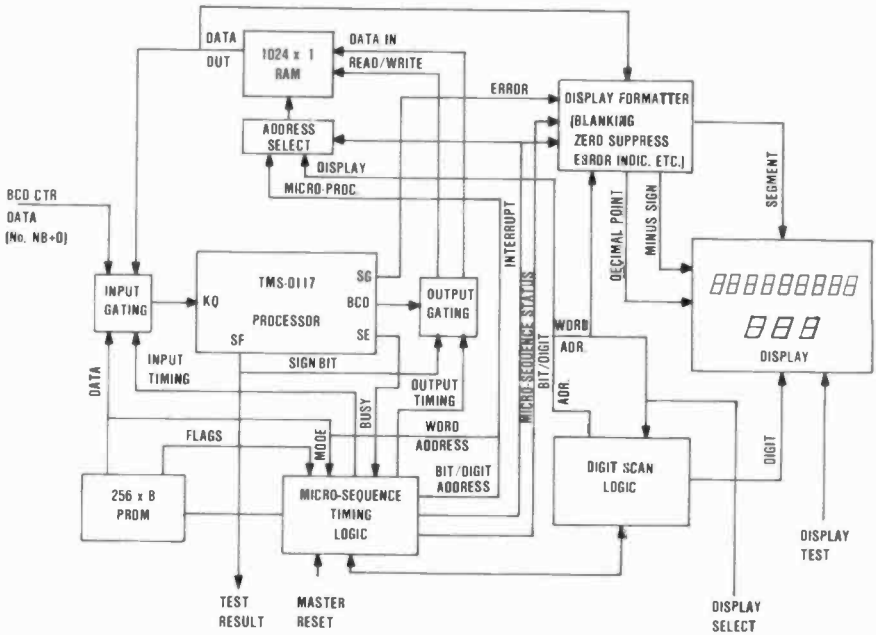


Fig. 17—One-way Doppler display approach.

−285,714.3 Hz when all components are working correctly. When converted to an equivalent S-band Doppler shift (× 221/192) the self-test signal will represent a Doppler shift of −328,869.05 Hz.

During the self test the microprocessor compares the actual measured Doppler with a stored value of −285,714.3 Hz. If the two frequencies agree within a few hertz, a "data-good" signal is sent to the 1218 computer and a data-good indication lights on the front panel of the extractor.

5.2 Microprocessor Hardware

The microprocessor circuits perform calculations on the BCD counter data to provide direct display of Doppler frequency (F_D), range rate ($\dot{R}$), change in range (ΔR), self-test error, and coincidence delay. The TMS-0117 was selected as the central processing element in a special-purpose microprocessor arrangement, since commercial microprocessors do not have a nine digit BCD capability.

Fig. 17 shows the microprocessor and display approach. The TMS-0117 functions as a central processing unit. A random-access memory (RAM) provides storage of intermediate and final calculation results. A programmable read-only memory (PROM) holds a series of instruc-

tions referred to as a microsequence or microprogram. The microsequence is the detailed set of data transfers and instructions required to compute the navigation parameters for display. The microsequence timing logic generates clock bursts used to operate the central processor, transfer data, and increment the microsequence memory. Input and output gating logic provides the multiplexing and serial–parallel conversion required to interface the TMS-0117 with the RAM, ROM, and extractor data registers.

This microprocessor approach has a speed disadvantage. Computation time for the navigation parameters is on the order of 1.8 seconds. Holding a number in the output registers of the TMS-0117 calculator chip would permit display of the output, but would tie up this chip during the display period. For this reason, the internal display scanning and blanking circuitry of the TMS-0117 was not utilized, permitting the chip to be used full time as a processor.

As shown in Fig. 17, separate display timing, formatting, and zero-suppression circuits are provided. The display logic shares the RAM with the microprocessor. In operation, the display circuits select and access the multiplexed display data by stepping through the appropriate block of RAM addresses. The microprocessor accesses the RAM on an interrupt basis, "stealing" the address and data leads to read or write a data word. The display is blanked during this interrupt. Upon completion of the interrupt, the RAM address and data leads are switched back to the display control circuits, where display scanning is resumed. Due to the low duty cycle of the interrupt action, the display appears undisturbed to the eye.

The RAM addressing is organized such that the microprocessor accesses one portion of the memory while the display logic accesses another. Intermediate calculations and new parameter results are stored in one half of the memory. Previously calculated results are stored in the other half. The display logic only accesses previous results, while both current and previous results are used by the microprocessor.

A strobe from the interval timer initiates the microsequence. Upon receipt of the strobe, the microprocessor will access the BCD data from the extractor and calculate all navigation parameters, storing the results in the RAM. At the completion of the microsequence, a bit of the RAM address will be inverted. This inversion has the effect of interchanging the new and old data within the RAM, so that the just-completed calculations appear on the display, while the other half of the memory becomes available for the next set of calculations.

This approach provides a sample-and-hold type of display, and permits viewing of previous calculations while new parameters are being calculated. With integration periods of less than 2 seconds, the microprocessor will be constantly calculating, necessitating the sample-and-

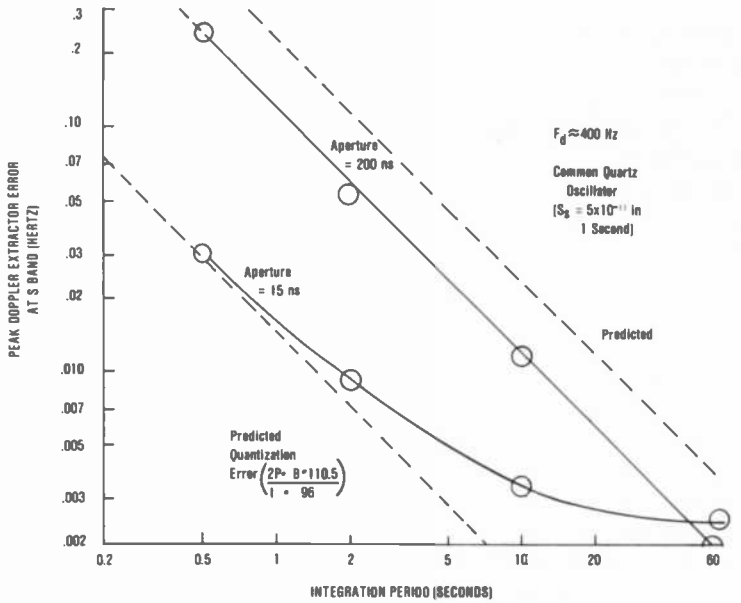


Fig. 18—One-way Doppler extractor measurement error.

hold display.

The microsequence is implemented without branching. Address registers and logic normally provided for this function are not required for this microprocessor.

6. Performance

6.1 Doppler Extractor Accuracy

Fig. 18 shows the test results of the sensitivity of Doppler accuracy to integration time and coincidence detector aperture (twice the pulse width). The results indicate that the extractor is capable of measuring the S-band Doppler to an accuracy of 0.03 Hz or better if aperture widths of 15 ns are used. This error is primarily caused by the quantization error for short averaging intervals, as shown by comparison with the expected quantization error. At long averaging intervals (>5 seconds), the error is greater than the expected quantization error, primarily due to clock and reference-frequency instability. With an aperture of 180 ns, the accuracy degrades to about 0.3 Hz in a 0.5-second averaging period. For comparison, a conventional zero-crossing counter would normally have a peak error of 2 Hz in a 0.5-second averaging period. Measurements of Doppler accuracy with apertures less than 15 ns were not made, although

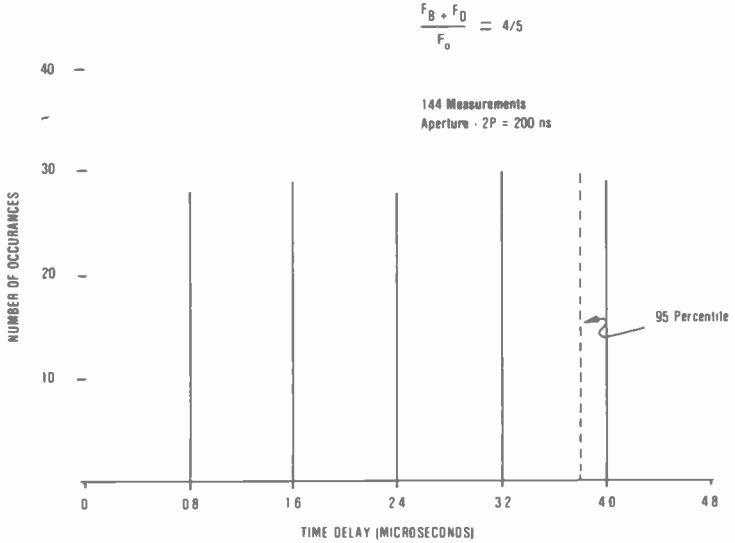


Fig. 19—Distribution of delay time.

the breadboard was designed to operate with an aperture as low as 2 ns. Had this aperture been used in the measurements, the expected peak quantization error would be 0.008 Hz in a 0.5-second averaging period.

6.2 Time Delay Statistics

The peak time delay between command and actual start of the counters, or time between coincidences, is sensitive to the aperture width and the ratio of the bias frequency to clock frequency (N/M).

Fig. 19 shows the statistics of the time delay for an aperture of 200 ns. The delay is uniformly distributed with a maximum of four microseconds. As the aperture is decreased, the distribution of delays appears to follow a Rayleigh distribution with large values of delay occurring rarely. At an aperture of 15 ns, very large delays are common. With this aperture, delays above 30 milliseconds occur half of the time.

Fig. 20 shows the sensitivity of the 95 percentile value of time delay to the aperture width. The results show a nearly linear relationship between the logarithm of the time delay and the value of the aperture width.

As the Doppler shift changes from the highly resonant condition of zero Doppler, the time delays decrease rapidly. For example, at an aperture of 15 ns, the 95 percentile time delay is about 50,000 μs at zero Doppler. However, at a Doppler offset of less than 500 hertz, the 95

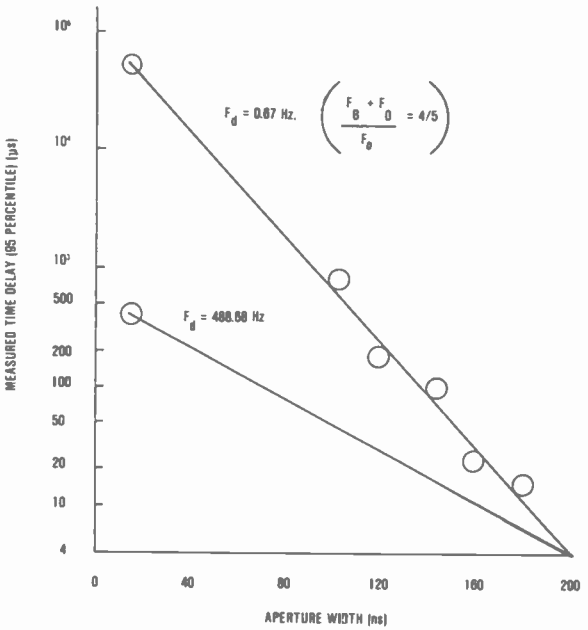


Fig. 20—Sensitivity of time delay to coincidence aperture and Doppler off-set.

percentile delay decreases to only 300 μs.

If a Doppler rate is present when the Doppler shift is near zero, the zero Doppler resonant condition would be short lived. For example, a Doppler rate of 1 kHz/second would cause a shift from +500 Hz of Doppler to −500 Hz in 1 second. Thus, the resonance would not last more than one second and time delays in excess of 300 μs would occur only rarely, even with aperture widths of 15 ns.

Acknowledgment

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Arnold R. Moore received his B.S. in Chemistry from the Polytechnic Institute of New York in 1942, with thesis work in chemical kinetics. Subsequently, he worked on gas discharge and photoelectric surface problems with the manufacturing devisions of RCA in Harrison, N. J., and Lancaster, Pa. In 1945, he returned to graduate school at Cornell University, where he received the Ph.D. degree in Experimental Physics, minor in Theoretical Physics and Mathematics, in 1949 under National Research Council Fellowship. His work at Cornell consisted chiefly of experimental research into the motion of electrons in alkali and silver halides, along with the growth of the required single crystals. He joined RCA Laboratories in 1949, working in the field of transistor physics, optical absorption in semiconductors and semiconductor alloys, magnetic susceptibility, acoustoelectric effect in cadmium sulfide and gallium arsenide, and most recently photovoltaic solar converters. In 1970–71 he was a visiting professor at Brown University where he taught a graduate course in physics of solid-state devices and participated in research on photovoltaic cells. Since in 1971, he has been Head of a group at RCA Laboratories working on insulators and photo devices. He has

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His work has centered on the optoelectronic and transport properties of solids, mostly semiconductors. He discovered the magnitudes and prevalence of natural electric fields in imperfect solids and their influence on a number of optoelectronic properties. That led to the first unified explanation for the character of the fundamental optical absorption edges of solids, the first comprehensive physical model for the operation of semiconductor lasers, and the identification of new mechanisms in electron–hole recombination in semiconductors. He developed a new technique for studying electronic transport in disordered semiconductors, and for several years has worked on properties of solar cell devices and systems. In 1974, he was granted an RCA Outstanding Achievement Award.

Dr. Redfield is a Fellow of the American Physical Society, was a member of the Executive Committee of its Division of Solid State Physics for 1973–1975. He is a Senior Member of the IEEE, a member of its Energy Committee, and Chairman of the Working Group on Energy/Environment of the IEEE Committee on Social Implications of Technology. He is a member of the Federation of American Scientists and was Chairman of the Princeton Chapter of FAS in 1971–1972, and a member of its Executive Committee in 1972–1973 and 1973–1974. He is a member of the Board of Editorial Associates of the new journal *Semiconductors and Insulators*.

Eugene R. Starner received his B.S. degree in Physics from Lehigh University in 1962, and has done graduate work at the American University in Washington, D.C. and the University of Pennsylvania in Philadelphia, Pa. From 1962 to 1967, he was engaged in studies for the U.S. Navy to determine the causes and techniques to reduce electromagnetic interference in the Navy's weapon systems. In 1967, he joined General Electric in Valley Forge, Pennsylvania where he worked on the design of digital filters for several earth satellite projects. In 1973, he joined RCA and began designing systems to extract range and doppler information from radio signals. He has been awarded several patents for these systems, including the One-Way Doppler Extractor system described in this issue of the RCA Review. He has recently been involved in the design of arithmetic frequency synthesizers for use in high-precision range and range-rate tracking systems.

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